DDS device produces sawtooth waveform

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Ramp or sawtooth waveforms are useful for a broad range of applications, including automatic-test equipment, benchtest equipment, and actuator control. Discrete components typically set the waveform frequency. Unfortunately, drift in these component values over time and temperature limits the accuracy of the output frequency. Also, changing the frequency requires that you use a different set of components. This Design Idea describes a flexible implementation of a sawtooth waveform generator (Figure 1) using two DDS (direct-digital-synthesis) devices. The frequency of the sawtooth is digitally programmable, so the design requires no external components to set the frequency. A DDS device, a programmable waveform generator, can deliver sine, square, and triangular (up/down ramp) waveforms. You can digitally implement changes in phase or frequency by loading onboard registers. Using the phase registers, the DDS chip can generate two linear up/down ramps of the same frequency but with a 90° offset. The up ramp of one occurs at the same time as the down ramp of the other. Selecting a phase register causes the signal from that register to go to the output. A sawtooth waveform occurs when the only the "up ramp" of each signal is directed to the output. The AD9833 delivers the MSB of the phase register, thus producing a digital signal at the frequency of the up/down ramp. This signal connects to the PSELECT pin on the AD9834, which controls switching between the phase registers.

Latency in the devices means that you see the effect of switching between the phase registers on the output only after seven MCLK (master clock) cycles. Controlling the MCLK signals of both devices so that one MCLK is inactive for a number of clock cycles can overcome this inherent latency. Figure 2 illustrates how the two devices connect. The connections to the interfaces of the two devices combine so that they can accept programs from the same digital controller. The AD9833 is connected such that FSYNC is active high; the AD9834 is connected such that FSYNC is active low. In this way, the controller has to control only three signals instead of six. The AD9834 is configured so that the frequency and phase are controlled via the pins. This configuration allows the digital output from the AD9833 to control phase-register selection by simply connecting it to the PSELECT line. Two analog outputs from the AD9834, IOUT and IOUTB, deliver complementary sawtooth waveforms (Figure 3).

A RESET (Pin 11) signal initializes the devices. This initialization can occur in the same way for both devices, using the control register. This operation requires a control word with the RESET bit set to 1. The frequency and phase registers of both devices are then ready to load with data. Because of the switching involved in creating the sawtooth waveform, its frequency is twice that of an equivalent triangular waveform.
\[ f_{\text{SAWTOOTH}} = \frac{F_{\text{WORD}}}{2^{27}} \times f_{\text{MCLK}}, \]

where \( F_{\text{WORD}} \) is the frequency word loaded in both devices.

The AD9834 phase switches between 0 and \( \pi/2 \). Following instructions in the IC’s data sheet, you should therefore load Phase Register 0 with 0 and Phase Register 1 with 0x800 (which corresponds to a 90° phase shift). The AD9833’s phase is always set to \( \pi/2 \), so you should therefore load Phase Register 0 with 0x800. Once the MCLK of the AD9833 begins to run and after seven MCLKs of latency, the output of the AD9833 changes because of the \( \pi/2 \) phase shift in Phase Register 0. You can deactivate RESET through the control register once the registers are loaded with data. In the same control word to the AD9834, you should set the MODE bit to 1, which results in the selection of the triangular waveform as the output waveform, and you should set PINSW to 1, so that the pin controls phase-register-select function. And, for the AD9833, you should set the OPBITEN bit to 1 to enable the digital output. You should set the DIV2 bit to 1 so that the digital output is not divided by 2, and set the SLEEP12 bit to 1 because the DAC is not being used. For the system to implement the sawtooth, there must be an offset between the times when the MCLKs of both devices begin to run. You calculate the offset as follows:

\[
\text{OFFSET} = \left[ \text{ROUND} \left( \left\lceil \frac{2^{28}}{F_{\text{WORD}}} \right\rceil \div 4 \right) - 7 \right].
\]

If, for example, Offset=10, then the MCLK of the AD9834 should run for 10 cycles before the MCLK of the AD9833 starts running. From then on, the ICs should be synchronous. A negative value of Offset indicates that the MCLK of the AD9833 should start running first.

This Design Idea provides a flexible method for generating a sawtooth waveform. The frequency is digitally programmable, and the design requires no external components to change the frequency. The frequency does not change with component drift over time or temperature.