This Design Idea shows a simple, low-cost circuit that produces a highly accurate variable-frequency and variable-duty-cycle output (Figure 1). Further, the duty cycle and frequency are independent of each other (excluding 0 and 100% duty cycle). The method derives its accuracy and stability from the fact that the output is based on a crystal oscillator and divisions of the oscillator's frequency. The design uses only six devices. IC1, a 74HC393 binary ripple counter, has as its input is the oscillator's output frequency. The outputs are the oscillator frequency divided by two, four, eight, 16, 32, 64, 128, and 256. IC5B is cascaded with IC1 to divide the oscillator frequency further by 512, 1024, 2048, and 4096. In this circuit, the divide-by-128 is the largest division it uses. You could, with a simple wiring change, substitute an unused divider to obtain a different output-frequency range. The eight inputs of IC2, a 74HC151 eight-line-to-one-line multiplexer, connect to the oscillator's frequency divided by one, two, four, eight, 16, 32, 64, and 128. Note that the oscillator's output connects directly to an input of IC2. This connection allows selecting the oscillator's frequency divided by one. IC2 connects one of the eight frequencies to the input of IC3.

IC3, a 74HC4017 decade counter, divides the frequency from IC2's output by 10. Therefore, the maximum output frequency for this design is the oscillator frequency divided by 10. Each of the decoded decade counter's 10 outputs goes high for one clock cycle only (Figure 2). Using the 10 outputs, a frequency's period divides into 10 equal intervals. You can use these 10 equal intervals to generate duty cycles of 10, 20, 30, 40, 50, 60, 70, 80, and 90%. For this circuit, the outputs of IC3, Q1 through Q8, yield the end-of-pulse signals for duty cycles of 10 through 80%, respectively. The start-of-pulse signal is Q9's negative edge, which occurs at the same time as Q0's positive edge. Therefore, you can use Q9 as start-of-pulse low true, and the end-of-pulse signals are high true. The eight inputs of IC4, an eight-line-to-one-line multiplexer, connect to eight of the nine end-of-pulse outputs from IC3. This circuit omits the 90% duty cycle. You can include the 90% duty cycle with a simple wiring change. If you want to select 0% duty cycle, connect an input to IC4. If you select 0% duty cycle, the generator's output is low. IC4 connects one of eight end-of-pulse signals to IC5.

IC5A is a binary ripple counter that serves as a set-reset latch. The start-of-pulse signal sets the latch. The end-of-pulse signal resets the latch. The output of IC5 is the variable-frequency and variable-duty-cycle output of the signal generator. For example, if the oscillator's frequency is 4 MHz and IC2's C B A inputs are 0 1 0, then the generator delivers 100 kHz. If IC4's C B A inputs are 0 0 1, then the generator's output exhibits 20% duty cycle. If you need to select from more than eight frequencies, use a larger multiplexer than IC2. Cascade more or different types of dividers to achieve your frequency needs. You can use a 74HC390 to obtain division by five, 10, 50, 100, and so on. If you need other duty cycles, cascade 74HC4017s to divide the period by the desired number of
intervals. Finally, if you need to select from more than eight duty cycles, use a larger multiplexer than IC4.