The circuit in Figure 1 performs active voltage-to-current conversion or acts as a variable-gain current mirror with high precision and bandwidth. A typical application is testing high-speed ICs or other devices that have inputs designed to be driven from current-steering DACs to enable a modulated voltage source to control the devices. The circuit thus simplifies the testing of such devices in isolation, because modulated voltage sources are readily available, but modulated current sources generally are not. A further use of the circuit could be for easy and precise control of a current-controlled, variable-gain amplifier by using an adjustable dc voltage source at the input.

Figure 1 shows the circuit configured as a voltage-to-current converter. The overall “gain” with the component values shown is 1 mA/V, but you can easily realize other gains by altering the component values. Note that the output of the circuit can both source and sink current.

Starting at the input, \( V_{IN} \), because the input of amplifier IC\(_1\) is at virtual ground, the parallel combination of \( R_1 \) and \( R_2 \) provides a 50Ω termination for the input signal. IC\(_1\) then inverts this signal with a gain of \( R_3/R_2 \). Amplifier IC\(_2\) provides a gain of \(-R_5/R_4\)=–1 to the signal received from IC\(_1\), but its noninverting input is tied to the 3V reference. Therefore, its output and the top of the current-sense resistor, \( R_6 \), is offset by 6V with respect to ground when \( V_{IN} \) is zero. The current source comprises amplifier IC\(_3\) and the p-channel JFET, Q\(_1\). The choice of a JFET, rather than a bipolar transistor, ensures very high speed, zero dc error, and almost perfect linearity in the output-current characteristic. The JFET is an SST175 from Vishay/Siliconix (www.vishay.com); it has a guaranteed \( I_{DSS} \) current of 7 mA, high speed, and low capacitance. Amplifier IC\(_3\) clamps the voltage at the source of Q\(_1\) and the bottom of \( R_6 \) at 3V. With no signal input, therefore, Q\(_1\) passes a constant quiescent bias current of 3 mA into the 3-mA constant-current sink involving IC\(_4\) and Q\(_2\). The output current of the circuit, which comes from the drains of Q\(_1\) and Q\(_2\), is zero. When \( V_{IN} \) assumes a level \( \Delta V_{IN} \) above ground, the voltage at the top of \( R_6 \) increases by the same amount. So the current through \( R_6 \) and, thus, the output current, \( I_{OUT} \), increases by an amount \( \Delta V_{IN}/R_6 \), equivalent to 1 mA/V.

This circuit differs from the traditional precision current-source topology (Figure 2) in that, the op amp in Figure 1 clamps the bottom end of the sense resistor at a constant voltage rather than being varied in response to the input signal. Instead, the voltage at the top end, which would normally be connected to a fixed voltage, varies in response to the input signal. Furthermore, because Q\(_1\) is always conducting, its gate-voltage variations are typically less than 200 mV in response to changes in \( V_{IN} \). The result is that no nasty current spikes transfer to the output via Q\(_1\)’s gate-channel capacitance when \( V_{IN} \) makes a step to or from zero. In a traditional circuit, because there is no current sink, the op amp must completely turn off the FET when the output current must be zero. In doing so, the op amp’s output slews several volts to saturation near its positive supply rail.
transferring a high-amplitude current spike onto the output. A spike of the opposite polarity and similar magnitude is created when the op amp has to recover from saturation and slew in the opposite direction to again turn on the FET.

The 3-mA constant-current sink comprises amplifier IC₄ and n-channel MOSFET Q₂. IC₄ clamps the voltage at the top of current-sense resistor R₇ at –3V. Because the voltage-reference circuit fixes the bottom of R₇ at –6V, the quiescent current through Q₁ remains steady at 3 mA, equal to the current through Q₁ when Vᵢᵣ is zero. When Vᵢᵣ assumes a level ΔVᵢᵣ below ground, the voltage at the top of R₆ decreases by the same amount; the current through Q₁ then falls below 3 mA; and the current sink obtains the balance of its current, ΔVᵢᵣ/R₆, from the load.

The –6V reference that fixes the bottom of R₇ derives from amplifier IC₅’s applying a nominal gain of –2 to the 3V reference. You should trim the –6V reference by means of Rᵥ₁, such that the output current is zero in the absence of an input signal; the quiescent currents in Q₁ and Q₂ are then equal. Note that this single adjustment entirely calibrates the signal path, canceling out the effects of resistor tolerance, amplifier dc errors, and any tolerance in the ±3V references but not the effects of finite open-loop gain. To ensure maximum bandwidth in the signal path, the amplifiers are AD8055ARs from Analog Devices (www.analog.com). These amplifiers can tolerate a total supply voltage of only 10V, so you must operate IC₁ from a split ±5V supply and IC₂ and IC₃ from a single-ended 10V supply, because their inputs are 3V above ground.

You can obtain optimum dc accuracy and stability by using an OP177GS amplifier for IC₄ and IC₅ and a high-quality reference IC, such as the AD780BR, for generating the 3V reference. You generate the –3V reference by applying a fixed gain of –1 to the 3V, using an inverting circuit similar to that used in Figure 1 for deriving the –6V reference. You should use 0.1% tolerance resistors where shown, and you can optionally include R₁₂ to provide 0.11% of additional gain to compensate for the finite open-loop gain of amplifiers IC₁ and IC₂. You can further optimize the dc stability by including R₁₅ and R₁₆, although the prototype does not use these resistors. In tests, without C₉, the bandwidth of the circuit with a 1V p-p sinusoidal input was 80 MHz when the circuit drove a resistive 100Ω load. The output rise and fall times with the same load and a 1V, 2.5-nsec input step are just 5.5 and 4.8 nsec, respectively, with no overshoot, as measured with a 500-MHz oscilloscope. The typical output compliance ranged from 1.7V to –2.8V. The maximum undistorted output-current swing extended from 0.1 to 2.1 mA.

For optimum frequency response and linearity, you should use the circuit to drive a virtual-ground load; in other words, you should use a high-bandwidth op amp configured as an current-to-voltage converter. If you use any other load, which must have low impedance in any case, and it is partly capacitive, you may need a small capacitor, Cₛ, across R₅ to optimize the overall transient response of the circuit at the expense of some speed. You can also configure the circuit to operate as a current-to-current converter with an overall gain of 0.1 mA/mA by omitting R₁₁, replacing R₅ and R₁₃ with 0Ω, and increasing the value of R₁₂ to 470 kΩ. You can use this configuration, for example, to scale the outputs from commercial current-steering DACs that typically have full-scale outputs in excess of those that ASIC inputs need. Thus, you could test an ASIC with current-driven inputs by using such a circuit between each input and each DAC output. Note that, in this configuration, amplifier IC₁ is configured as a current-to-voltage converter with a gain of 0.1V/mA and presents a virtual-ground to the DAC outputs, a load that normally ensures optimum linearity performance from the DACs. The circuit supports both current-sourcing and current-sinking DACs, because the circuit can source as well as sink current. For high-speed operation, you may need a small capacitor across R₅ to cancel the effect of the DAC’s output capacitance and any stray capacitance.