A VCO (voltage-controlled oscillator) is an analog circuit, so you cannot find it in the libraries for the design of digital programmable chips. When you need such a circuit for synchronization or clock multiplication, you need to find a circuit that works with the standard digital functions, such as AND and NAND. Several possibilities exist for building variable-frequency oscillators. For example, you can change the frequency using a varactor diode. Unfortunately, these diodes have a small change of frequency per volt. So, the standard Pierce oscillator with one inverter and capacitors is not useful for these applications. Another idea is to use a Schmitt-trigger inverter and to vary the charging resistor. This method can work, but the hysteresis of the IC usually has a wide tolerance, so the selected inverter chip has a large influence on the frequency.

For these reasons, this design modifies a two-NOR-gate RC oscillator (Figure 1) to function as a VCO. For almost all pure-CMOS circuits, the switching point between high and low states is approximately $V_{CC}/2$. This point does not depend on the device. Using this circuit, you can obtain a wide frequency-tuning range. The output is a square wave with a 50% duty cycle. At power-on, both capacitors $C_1$ and $C_2$ are uncharged, and IC$_{1A}$ has a low output. Thus, the output of IC$_{1B}$ is high, and $C_2$ charges with the time constant $R_2C_2$. The additional charging current from IC$_{ST}$ and $R_4$ also influences this charging time. When the voltage on $C_2$ reaches $V_{CC}/2$, IC$_{1B}$ switches to a low state. Now, the output of IC$_{1A}$ switches high, and $C_1$ charges with time constant $R_1C_1$, influenced by IC$_{ST}$ and $R_3$. The low signal at the output of IC$_{1B}$ forward-biases $D_2$ and quickly discharges $C_2$.

This circuit produces a 50% duty cycle if $C_1=C_2$, $R_1=R_2$, and $R_3=R_4$. The values of $R_4$ and $R_3$ and the steering voltage, $V_{ST}$, determine the VCO's gain in kilohertz per volt. The circuit in Figure 2 yields the highest possible value for the VCO's gain. The circuit uses an Altera (www.altera.com) EPLD (erasable programmable-logic device), the EPM3032. Tristate buffers replace the diodes in Figure 1, and the charging resistors connect directly to the steering voltage. This configuration produces the highest possible VCO gain: approximately 700 kHz/V for the component values shown. You can switch off the VCO by using a steering voltage lower then $V_{CC}/2$. You can implement this circuit using almost all programmable-logic devices with CMOS inputs. You can also use steering voltages much higher then the supply voltage of the programmable chip, because the voltage on the input of the chip never goes higher then $V_{CC}/2$. This fact makes the circuit suitable as a voltage-to-frequency converter with a high input-voltage range.