Board-level signal-integrity analysis: Sooner is better

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Hyperlynx's system is free if you're a semiconductor-company model developer and if the IBIS
undershoot, and crosstalk, you use a fast model with maximum currents and the fastest
models can also account for many nonlinear aspects of an I/O buffer's design, such as
and be sure to rerun analyses throughout and after completion of physical-board
measurements on a fully loaded pc board. Use your preroute SI analysis to guide your design,