You can estimate the parasitic series inductance of a bypass capacitor in a multilayer board with solid power and ground planes. Use an approximation for the inductance $L_1$ due to the chip layout (Figure 1, green shaded region). Then, assuming that you have connected your chip and your bypass capacitor straight to the planes, use an approximation for the inductance $L_2$ represented by the volume of magnetic flux trapped between the planes (blue region). Finally, you might want to consider the inductance, $L_3$, of the chip package itself (red region). The internal details of the construction of a monolithic ceramic capacitor add little to the total inductance.

The chip-package inductance (red region) is the least troublesome of the parts. Considering the chip's power and ground pins as a source of noise, the impedance of this source is much larger than the impedance between power and ground on your board. (If it were not, your board would have so much power-supply noise that it wouldn't work.) Therefore, the chip tends to act as a fixed source of current, independently of $L_3$. In other words, $L_3$ affects the power-and-ground bounce that your chip experiences but not the noise coupled onto the power and ground planes.

The chip power-supply currents flowing through the impedances of $L_2$ and $L_1$ generate most of the high-frequency power- and ground-plane noise emanating from the structure in Figure 1. Power- and ground-plane noise in the frequency region that the bypass capacitors control is therefore proportional to $L_2 + L_1$. To compute $L_2$ (blue region), assuming that the field intensity generated between the planes due to a single via with diameter $D$ falls off inversely with distance and is independent of height, use $L_2 = (\mu_0 / p)(H_2 \ln(2S_2 / D))$. With $H_2$ in inches, the quantity $\mu_0 / p$ equals 10.16 nH.

The $L_1$ computation (green region) first divides into the part of the inductance due to the capacitor body and pads and then divides the part due to the vias. The combination of body, surface-mounting pads, and via pads (assuming that the vias are jammed right up against the mounting pads) comprises a long, wide structure that resembles a transmission line. For example, a 0603 mounting structure is approximately 30 mils wide, 120 mils long (via center to via center), sitting at some height, $H_1$, above the nearest solid reference plane. Given the characteristic impedance, $Z_0$, for a structure with this width and height, and the time delay, $T$, corresponding to its length, you may approximate the inductive contribution due to the body and pads (ignoring fringing fields at the ends) as $L_1$ (body) = $Z_0 \cdot T$. You can use any ordinary transmission-line calculator to approximate $Z_0$ and $T$. Next, approximate the inductive contribution of the vias at the ends using the Biot-Savart law integrated over the blue region, assuming the vias represent tiny current elements. The result is $L_1$ (vias) = $(\mu_0 / 2p)'(H_2^2)(2/D - 1/S_1)$. Add the two contributions to find the total, $L_1$. This approximation works only when $S$ is larger than $D$. 

Parasitic inductance of a bypass capacitor

Howard Johnson - December 31, 1969
Figure 1 graphically depicts calculations for a 0603 layout, with the vias jammed up against the capacitor mounting pads. The figure shows the total inductance, $L_1$, versus height. The assumed pad width is 30 mils, the total structure length (via center to via center) is 125 mils, and the via diameter is 12 mils. The x-marks show actual measured results. The value of $L_2$ for this structure, assuming $S_2 = 0.500$ and $H_2 = 0.005$ is 0.22 nH. Both $L_1$ and $L_2$ vary strongly with height.

If you mount the capacitor on the reverse side of the board, you have to sum the various inductances $L_{2A}$, $L_{2B}$, and others (yellow regions), thus illustrating the disadvantage of backside mounting.

If you must use traces to connect the capacitor vias connect to the capacitor mounting pads, add the inductance of those traces to $L_1$. At roughly 10 nH/in. for typical pc-board traces, the extra trace inductance quickly adds up. For example, 0.050-in. long traces at each end of a standard 0603 component adds around 1 nH to the completed layout inductance, substantially raising $L_1$.

Author Information