Bypassing PC boards: Thumb your nose at rules of thumb

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The need for effective and efficient bypassing has grown as a consequence of shrinking power-supply voltages and expanding requirements for bypass networks that work from kilohertz to hundreds of megahertz. Bypassing strategies are often based on rules of thumb. Although such approaches may have worked in the past, they don't satisfy today's increasingly difficult requirements. To help you meet those requirements, this design feature:

- presents a technique that you can use to design a decoupling strategy that meets specific system requirements,
- makes you aware of such issues as parasitic elements and bypass components' imperfect nature,
- presents a means for accommodating larger pc boards' high-frequency behavior as 3-D transmission lines,
- provides an equivalent lumped-parameter model for the pc board, and
- identifies some pitfalls of arbitrarily applying rule-of-thumb design practices.

A typical power-supply output filter consists of a 330-µF electrolytic capacitor (Figure 1). Although the capacitor is not a particularly good choice because it provides poor decoupling above 1 MHz, it illustrates the crux of the decoupling problem: You have to work with nonideal components, and you must overcome the transmission-line effects of the "raw" pc board. Worked examples illustrate the concepts.

![Figure 1](image)

**Figure 1** Although an ideal capacitor would have an impedance-versus-frequency characteristic that declines monolithically at 20 dB/decade, parasitic resistance and inductance give a real capacitor a resistive (zero-slope) characteristic at intermediate frequencies and rising (inductive) impedance at higher frequencies.
Modeling capacitors

A model for practical capacitors consists of a series-resonant circuit (Figure 2). The parasitic elements are the ESR and the ESL (equivalent series inductance). Table 1 provides measured data (the average of 10 units) for some typical surface-mount decoupling capacitors. In Figure 3's model for a typical surface-mount capacitor, you must add the inductance of the leads, \( H_1 \) and \( H_2 \), to the device's ESL.

![Figure 2](image)

**Figure 2** The series-equivalent circuit of a real capacitor includes a resistor and an inductor, as well as the capacitor.

<table>
<thead>
<tr>
<th>Type</th>
<th>( C ) (( \mu )F)</th>
<th>ESR (( \Omega ))</th>
<th>ESL (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrolytic</td>
<td>330</td>
<td>0.1</td>
<td>5</td>
</tr>
<tr>
<td>Tantalum</td>
<td>4.7</td>
<td>0.8</td>
<td>1.6</td>
</tr>
<tr>
<td>Ceramic</td>
<td>0.1</td>
<td>0.18</td>
<td>1.0</td>
</tr>
<tr>
<td>Ceramic</td>
<td>0.01</td>
<td>0.29</td>
<td>1.8</td>
</tr>
</tbody>
</table>

1 Does not include trace inductance.

![Table 1](image)

**Table 1**—Surface-mount capacitor parameters

![Figure 3](image)

**Figure 3** Besides the three elements that represent the capacitor itself, a surface mount capacitor's circuit model includes elements that represent the inductance of the traces that connect the capacitor to the rest of the circuit.

Primarily because of their low ESR, ceramic capacitors are often regarded as superior at high frequencies to tantalum capacitors. However, for decoupling, you can use the tantalum capacitor's
ESR to dampen the resonances that result from interaction between the capacitors’ ESLs and the PCB board’s various capacitances. The high ESR acts as a built-in damping resistor and makes the tantalum capacitor a good choice for decoupling.

Figure 4 illustrates the primary difference between ceramic and tantalum capacitors. Notice the tantalum capacitor’s relatively large resistive band compared with that of the ceramic device. As long as all of the decoupling capacitors have equal capacitance, the corner frequencies of the resistive band do not change as you change the number of parallel capacitors (Figure 5). In some cases, it is desirable to shift the frequency range of the resistive band. Figure 6 compares the impedance of a single 4.7-µF tantalum capacitor with that of 14 0.33-µF tantalum capacitors in parallel. Although their total capacitance is about the same as that of the single capacitor, the 14 capacitors have a resistive band that is higher in frequency.

**Figure 4**
A 0.1µF ceramic capacitor’s impedance-versus-frequency characteristic shows almost no resistive region, whereas the characteristic of a 4.7-µF tantalum capacitor displays a resistive region that covers more than two decades of frequency.

**Figure 5**
Increasing the number of nominally identical capacitors that you place in parallel has no effect on the frequency range over which the devices appear resistive but does affect the ESR.
Replacing one 4.7-uF tantalum capacitor with 14 0.33-uF capacitors in parallel yields about the same capacitance but lowers the ESR and raises the resistive region's frequency range.

### Modeling pc boards

A pc board's power planes constitute a nonterminated, lossless, 3-D transmission line. With respect to power-supply (V\(_{CC}\)) decoupling, the pc board's transmission-line effects are significant in many cases, and you should consider them. Figure 7 shows the impedance of a 9X10X0.003-in. pc board.

The succession of peaks and valleys in the impedance-versus-frequency plot of a 9x10x0.003-in. pc board reveals the distributed (transmission-line) nature of the board as a circuit element.

Numerous resonance points characterize the transmission line. Of particular importance is the first resonance point at \(f_0\). An equivalent series-resonant circuit approximates the pc-board impedance at frequencies as high as \(f_0\) (Figure 8).
Figure 8 The simplest equivalent circuit of a transmission line treats the line as if it exhibits no series impedance and exhibits only a shunt impedance (a capacitor in series with an inductor) between the pair of conductors.

Higher order models model the pc board to the second resonance point, $f_1$, and beyond. However, for most cases, modeling the pc board to $f_0$ is sufficient. For a 3-D pc board, $C_S$, the dc-transmission-line capacitance, is given by:

$$C_S = (\varepsilon_0 \times \varepsilon_r \times \text{Area IN.}^2 / \text{h IN.})2.54 \times 10^{-2}$$  \hspace{1cm} (1)$$

where $\varepsilon_0$ is the permittivity of free space, $\varepsilon_r$ is the dielectric constant (also known as "relative permittivity"), and $h$ is the board thickness in inches.

The ESL, $L_S$, is

$$L_S = 1/C_S \times 2\pi f_0^2$$  \hspace{1cm} (2)$$

To solve for $L_S$, you must determine the raw pc board's principal resonant frequency. This frequency is a function of the test point's location on the pc board. Equations for predicting the principal resonance at the center, side, and corner of a rectangular pc board have been determined empirically, and these equations follow.

$$f_0 \text{(CENTER)} = 1.43 \times 10^9 / \sqrt{\text{AREA}}$$

$$f_0 \text{(SIDE)} = f_0 / \sqrt{2} = 1.43 \times 10^9 / \sqrt{2}\text{AREA}$$

and

$$f_0 \text{(CORNER)} = f_0 / \sqrt{4} = 1.43 \times 10^9 / \sqrt{4}\text{AREA}$$  \hspace{1cm} (3)$$

The speed of propagation within the pc board, $c_{\text{PCB}}$, is independent of the dielectric thickness and is proportional to $\sqrt{\varepsilon_r}$. Typical pc-board materials have an $\varepsilon_r$ of 4.6 to 4.8, so $c_{\text{PCB}}$ is approximately equal to 2.15 nsec/ft (versus ;1 nsec/ft in free space). Although $c_{\text{PCB}}$ is independent of the board dimensions, $Z_0$, the characteristic impedance of the transmission paths within the board, depends
strongly on the dielectric thickness and trace width.

For illustration, assume that the pc board has an area of 9X10 in., a dielectric thickness of 0.003 in., and a dielectric constant of 4.6. The worst-case (lowest frequency) principal resonance occurs when you look into a corner of the pc board. Therefore, from Equation 3, the principal resonance is:

\[ f_0 \text{ (CORNER)} = 1.43 \times 10^9 \frac{1}{\sqrt{2 \text{AREA}}} = 1.43 \times 10^9 \frac{1}{2\sqrt{9 \times 10}} = 75 \text{ MHz} \]  

\[ (4) \]

From Equation 1, the total dc capacitance is:

\[ C_s = (\varepsilon_0 \varepsilon_r \text{ Area IN.}^2 \div \text{h IN.}) 2.54 \times 10^{-2} = (8.9 \times 10^{-2})(4.6)(9 \times 10)(0.0254)/0.003 = 0.03 \text{ uF} \]

And, from Equation 2, the ESL is:

\[ L_s = \frac{1}{C_s 2\pi f_0^2} = \frac{1}{0.03 \text{uF}(2\pi 75 \text{ MHz})^2} = 150 \text{ pH} \]

Figure 9 shows the impedance of both the raw pc board and the equivalent LC model. As mentioned, the LC circuit approximates the pc board to \( f_0 \).

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**Figure 9** The two element LC transmission line model is surprisingly accurate at frequencies below and including the first resonant frequency \( f_0 \).

You can now construct the decoupling model (Figure 10). This model includes the power-supply capacitor, power-entry impedance, raw-pc-board parasitic circuit elements, and decoupling capacitors. The power-entry impedance is the impedance of the wiring between the power supply and the pc board's power planes. This impedance includes the series inductance of power feeds and jumpers. You can model the pc-board-mounted devices (ICs) as a current-noise source that drives the overall pc-board impedance. Therefore, the goal of the decoupling strategy is to keep the pc-board impedance low to minimize the induced noise voltage. Unfortunately, the noise-current spectrum is generally unknown. Therefore, predicting the exact impedance requirements is impossible.
The network includes the power supply, the power-entry wiring, the "raw" pc board, the board-mounted components (ICs) and the decoupling capacitors. The circuit model includes mostly RC and RLC networks between the supply buses. A series inductor simulates the power-entry wiring. A noise-current source represents the ICs, which draw transient currents when they switch.

To illustrate, assume that the impedance requirement at the pc board's power-entry point at the corner of the board (as described by Equation 4 in the previous example) is: $Z_{IN}=0.1\ \text{Ohm}$ from 10 kHz to 200 MHz. Recognizing that tantalum capacitors offer some advantage over ceramic capacitors for decoupling, you elect to use 15 4.7-µF tantalum capacitors. Figure 11, which ignores the power-entry impedance, $Z_{PE}$, shows the composite impedance of all of the parallel circuit elements as well as the individual impedances of the power-supply capacitor (330-µF electrolytic, $Z_{PS}$), the decoupling capacitors (15 4.7-µF tantalums, $Z_{dp}$), and the raw 9X10X0.003-in. pc board ($Z_{PCB}$).

The impedance-versus-frequency plot of all the shunt passive networks in parallel shows that, from approximately 30 kHz to 200 MHz, the decoupling limits the impedance to no more than 0.1 Ω.
The figure shows that the design meets the 0.1 Ohm goal over the required frequency range. The peaking that occurs near the pc board's principal resonance is the result of the bypass capacitors' ESL intersecting with the pc board's capacitance. (That is, at the resonant frequency, the magnitude of the ESL's inductive reactance equals that of the pc board's capacitive reactance.) The tantalum capacitors' resistive band effectively dampens this resonance.

**Maximum power-entry inductance**
You must still determine the maximum allowable power-entry inductance. In many cases, adding an inductance improves the bilateral isolation (that is, isolation in both directions) between the power distribution and the power planes. The largest power-entry inductance provides the greatest isolation. You cannot make this value arbitrarily large, however. To minimize peaking, the value must be small enough that the power-entry impedance intersects the decoupling-capacitor impedance in the resistive (real) band. The inductance that intersects the corner of the resistive band is the "corner inductance."

For this example, the corner inductance is $L_{\text{CORNER}}=800 \text{ nH}$ (Figure 12). The power-entry inductance ratio, $k$, is the ratio of the corner inductance to the actual power-entry inductance, $k=L_{\text{CORNER}}/L_{\text{PE}}$. Figure 13 shows the voltage-transfer functions from the power supply to the pc board for various inductance ratios. Peaking in the transfer function occurs between 10 and 400 kHz. This range is typical for the power supply's switching frequency. Therefore, any peaking in the transfer function could increase the power-supply ripple that the pc board sees. To keep the peaking relatively low (less than 2 dB), $k$ should be no less than 10. For this example, if $k=10$, the maximum power-entry inductance is: $L_{\text{PE}}=L_{\text{CORNER}}/10=800 \text{ nH}/10=80 \text{ nH}$.

![Figure 12](image)

**Figure 12** The inductance ratio, $k$, is the ratio of the corner inductance to the power-entry inductance. The corner inductance is the inductance whose reactance magnitude equals that of the model's parallel shunt passive networks at the frequency at which those networks begin to appear resistive.
Increasing $k$ increases the damping (reduces peaking) in the voltage-transfer ratio from
the power supply to the pc board.

For $k=10$, the voltage-transfer function from the pc board to the power supply appears in Figure 14. For this example, the power supply is isolated from the pc board for frequencies greater than 200 kHz. The isolation is especially important when a power supply connects to more than one pc board. In this case, it is desirable to keep the noise of each pc board from feeding back onto the distribution bus.

If $k = 10$, the voltage-transfer ratio from the pc board to the power supply shows little
peaking. This plot shows voltage transfer for noise generated on the pc board. The direction is
opposite that Figure 13.

At this point, the decoupling model is complete. A plot shows the composite impedance for the
power-supply, power-entry, and bypass elements and for the pc board (Figure 15). The 15 4.7-µF
tantalum capacitors meet the 0.1 Ohm design requirements from 8 kHz to 200 MHz.
Figure 15 Adding the impedance between the power supply and the pc board changes the shape of the shunt-impedance-versus-frequency curve (Note the curve labeled “composite”)

For decoupling, it is generally best to use the smallest practical pc-board dielectric thickness. To illustrate, consider increasing the dielectric thickness from $h=0.003$ in. to $h=0.03$ in. The change decreases the pc-board capacitance by a factor of 10 but also increases the pc-board inductance by a factor of 10. Because the capacitance decreases by the same amount that the inductance increases, the principal resonance remains unchanged. In other words, the principal resonance is a function of the dielectric constant and the surface area of the pc board, but not of the dielectric thickness.

Figure 16 shows the composite impedance for the power supply, power entry, and 15 4.7-µF tantalum decoupling capacitors. Curves show the impedance for $h=0.03$ in. and $h=0.003$ in. With $h=0.03$ in., decoupling degrades (impedance increases) near the principal resonance. As the pc board’s dimensions increase, the principal resonance decreases in frequency (moves to the left). Therefore, for very large pc boards, the raw pc-board effects are more significant.

Figure 16 Increasing the pc board thickness from 0.003 in. to 0.03 in. doubles the shunt impedance (that is, reduces the decoupling’s effectiveness) at frequencies greater than about 80 MHz

Pitfalls of rule-of-thumb design

The following example illustrates some of the pitfalls of using the rule-of-thumb approach. In
particular, it is common to "sprinkle" ceramic capacitors around the board. Typically, this approach calls for a 0.1- or 0.01-\(\mu\)F ceramic capacitor for each IC. Following this rule, assume there are 45 0.1-\(\mu\)F ceramic capacitors for the 9X10X0.003-in. pc board described earlier.

Figure 17 compares the design approach in the previous section with the rule-of-thumb approach. The decoupling-by-rule-of-thumb design does not meet the specified requirement (0.1 Ohm from 10 kHz to 200 MHz). Decoupling is worst at two frequencies: when the reactance magnitude of the power-entry inductance equals that of the decoupling capacitors and when the reactance magnitude of the decoupling capacitors' ESL equals that of the pc-board capacitance.

![Figure 17](image)

**Figure 17** Decoupling based on a rule-of-thumb approach yields a shunt impedance that varies much more with frequency than does the impedance that results from a rigorous approach. Worse yet, the rule-of-thumb approach yields an impedance that exceeds the design requirements at low and high frequencies

References


Author's biography

Jeffrey Pattavina is director of technology for Intraplex Inc (Middletown, CT), where he develops new technologies and products. He holds a BSEE from the University of Massachusetts—Amherst and an MSEE from Northeastern University (Boston). In previous jobs, he worked on many wire-line communication products and technologies, including integrated-services digital networks and HDSL.