06.18.98 Hot swap shrinks CompactPCI downtime

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Thanks to Joe Pavlat of PLX Technology for his valuable insight. Northern Telecom, Motorola Computer Group, Amp, and Teknor Industrial Computers are responsible for the development of the desktop PCI bus, CompactPCI allows designers to take advantage of off-the-shelf PCI technology. The popularity grows, a new hot-swap specification boosts system reliability for competition in the networking arena.

CompactPCI is a hardware-connection controller that can disable a malfunctioning board and replace it with a new one. Basic hot swap works with PCI-bus-interface silicon and Windows NT.

Full hot swap requires I/O switch chips with a built-in in-memory register that enables the operating software automatically identify the inserted board. With full hot swap, you can replace a failed board without turning off the system, and the operating software is responsible for the board’s new PCI resources.

Real-time hot swap requires the operating system to monitor the PCI signals at all times and be aware of the inserting PCI cards. The most critical technology necessary for hot swap is the software. The operating system must be aware of the board’s address, and interrupt assignment, during a hot-swap event while the remainder of the system is functioning normally.

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The software requests the hardware to terminate all PCI operations, and the hardware sends a terminal request to the I/O switch. The board front-panel LED illuminates to tell you that the board is safe for removal. When you install the new board, the ejector switch tells the operating software to automatically identify the defective board and follow with board shutdown. The board front-panel LED illuminates to tell you that the board is safe for removal. When you install the new board, the ejector switch tells the operating software to automatically identify the defective board and follow with board shutdown.

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- A new hot-swap specification puts CompactPCI to work in the booming telecommunications industry.
- Hot-swap-compatible PCI-bus-interface silicon is available for new CompactPCI adapter-board designs.
- CompactPCI hot swap leverages the PCI SIG hot-plug software for immediate operation with Windows NT, NetWare, and Unix-Ware.

What is PICMG anyway?

Four computer vendors formed the PCI Industrial Computer Manufacturers Group (PICMG) in 1994 as a consortium to standardize the use of ISA- and PCI-bus products. The group immediately began work on CompactPCI, a tactical initiative comprising six member companies producing the first CompactPCI specification in November 1995. PICMG comprises 389 member companies with affiliate organizations in China, Japan, and Europe. In addition to the core CompactPCI specification, PICMG technical committees are working on 11 auxiliary CompactPCI specifications including hot swap, which defines pin sequencing, hardware technologies, and the software architecture to support live insertion and extraction of boards in a CompactPCI system.

The PICMG specifications under development are:

- PICMG 2.1 CompactPCI hot swap defines pin sequencing, hardware technologies, and the software architecture to support live insertion and extraction of boards in a CompactPCI system.
- PICMG 2.2 VME64x bus pin assignments on CompactPCI defines pin assignments for the VME64x extensions, as standardized under the auspices of ANSI and the VME International Trade Association (VITA) on J5/P4 and J5/P5 of a CompactPCI backplane.
- PICMG 2.3 PMC I/O pin assignments on CompactPCI defines user I/O-pin mappings from IEEE 1386 PMC sites to J3/P3, J4/P4, and J5/P5 on a CompactPCI backplane.
- PICMG 2.4 IP I/O pin assignments on CompactPCI defines user I/O-pin mappings from ANSI/VITA standard IP sites to J3/P3, J4/P4, and J5/P5 on a CompactPCI backplane.
- PICMG 2.5 CompactPCI computer-telephony defines pin assignments for the computer-telephony functions of standard time-division-multiplexed buses, telephony rear I/O, 48V dc, and ringing distribution in a 6U chassis.
- PICMG 2.6 PCI-to-PCI bridging for CompactPCI backplanes defines the bridging of two CompactPCI local buses in one slot in a 6U environment.
- PICMG 2.7 dual CompactPCI backplanes defines a means for CompactPCI CPU boards to drive two independent PCI buses in a 6U environment.
- PICMG 2.8 secondary system-management bus for CompactPCI defines a secondary system-management bus to allow the host or other subordinate processors to interrogate and control CompactPCI cards.
- PICMG 2.9 secondary power connector removes the current power-connector requirement from the base specification and expands it to include new technologies.
- PICMG 2.10 keying for CompactPCI boards and backplanes defines the keying mechanisms in IEC 1076-4-101 for the J4/P4 connector and in IEEE 1101.10 for handle and card-guide hardware.
- PICMG 2.11 front-access power connectors removes the current power-connector requirement from the base specification and expands it to include new technologies.