SOC vs. SOP: And the Winner Is...

Kelly Barrett - May 28, 2001

While semiconductor device experts often view system-on-a-chip (SOC) as the greatest thing since the IC, many packaging researchers expect it to have cost issues down the home stretch. A number of packaging gurus will explain why they think novel packaging solutions such as system-on-a-package (SOP) will be the odds-on cost favorite at the Electronic Components and Technology Conference (ECTC), to be held in Lake Buena Vista, Fla., May 29-June 1.

Intel researchers look to improve throughput and costs for BGA packages by screen-ball printing. This process screens solder paste on the substrate to form the balls, rather than using the conventional process of fluxing the surface and placing preformed solder balls. Details will be presented at this week’s ECTC conference in Lake Buena Vista, Fla.

"The concept of system-on-a-package was born when the packaging community began to question the claimed technical justifications for SOC," said Evan Davidson, distinguished engineer, IBM Corp., Poughkeepsie, N.Y. Although SOC has been the approach of choice for digital applications up to this point, Davidson expects that situation will change to favor SOP.

In the future, two of the applications currently using SOC—microprocessors and wireless handsets—are likely to become more expensive, and the single-chip solution may not pass muster of a business-case analysis, according to Davidson. "Partitioning the SOC functions and placing them onto small few-chip modules can result in a lower system cost with no performance sacrifice," he said.

Davidson will be presenting his SOC vs. SOP analysis at ECTC. Other packaging talks will be given by researchers from Intel, Fairchild Semiconductor, Nokia, Toshiba and many other companies and
academic institutions. Conference details are available at the [www.ectc.net](http://www.ectc.net) Web site.

The conference underscores the packaging mantra of smaller-cheaper-cooler products by offering discussions on new package and process developments.

Wayne Howell of IBM is program chairman for the 51st Electronic Components & Technology Conference (ECTC).

"We will see a heavy emphasis on system-on-a-package, including chip stacking, wafer-level packaging, chip-scale packaging and multichip modules," said Wayne Howell, ECTC program chair and senior technical staff member and manager of business and technical strategy, IBM, East Fishkill, N.Y.

"The industry thrust that's driving many of the papers this year involves requirements for higher levels of integration and performance that are packaged in smaller form factors at much lower costs," Howell said. Possibly the industry segment seeing most of the pressure for less expensive, denser packaging is the mobile-product market.

Nokia researchers Seppo Pienimaa and Nigel Martin will be discussing how the use of flip-chip, chip-scale packages, high-density printed-wiring boards and integrated passive devices permitted a 50 percent area reduction of their mobile products.

"We have demonstrated that with careful packaging-technology selection it is possible to make dramatic reductions in the size of the electronics in a mobile terminal," the Peinimaa-Martin paper states.

While packaging options are being analyzed for size reductions, manufacturing processes are also being scrutinized for cost reductions. Y.T. Chin and his colleagues at Intel Corp. in Malaysia will present a paper that reviews a low-cost screening process to form balls on BGA packages.

Chin's paper identifies modifications that are needed to conventional screening processes to repeatedly form properly sized balls. In addition to reducing the amount of flux used, a different solder paste is required to reduce the incidents of ball bridging and so-called "monster ball" defects, the paper states. Higher throughput and lower costs are the two motivators for why Intel (nasdaq: INTC) is looking into screen-ball printing.

Cost is also the main thrust of another paper being given by Intel engineers. Tee-Onn Chong and his colleagues will give a talk on "Low-Cost Flip-Chip Package Design Concepts for High-Density I/O."

Clever flip-chip packaging designs will also be discussed by researchers who were looking for a better way to cool their power transistors. Fairchild Semiconductor Corp. engineers Rajeev Joshi, Romel Manatad and Consuelo Tangpuz helped develop the flip-chip in a leaded molded package, which is offered in a standard, eight-leded surface-mount package.
The ECTC is sponsored by IEEE; Components, Packaging & Manufacturing Technology Society; and The Electronic Components, Assemblies & Materials Association, which is the components sector of the Electronic Industries Alliance.