Teradyne Inc. today announced Hynix Semiconductor Inc. has evaluated high-speed wafer test at its facility in Ichon, South Korea, using a Teradyne wafer probe system.

Boston-based Teradyne (nyse: TER) said the evaluation was done to lay the groundwork for expanded sales of DRAM bare die and increasing use of wafer-level chip scale package (CSP) applications. Bare die chips are unpackaged devices typically used in multi-chip modules (MCM) for communication and consumer applications, such as cell phones, PDAs and digital cameras. Teradyne said Semico Research of Phoenix predicts DRAM consumption in these products will grow at nearly double the rate of the computer related applications over the next few years, achieving nearly 55 percent of the DRAM market by 2005.

"Today most DRAM bare die are sold without being tested at full array speed," said Joo Young Lee, memory product manager at Teradyne. "Test speed at wafer probe has been limited to 60MHz or less by insufficient timing accuracy, along with narrow probe card bandwidths and interface technologies that hinder signals between the channel card and wafer."

Teradyne claims Hynix’s use of its J996FA 125MHz wafer probe system is significant as testing at low frequencies like 60MHz does not guarantee a device will perform correctly in the final application.

"The J996FA with its high-bandwidth interface and FormFactor probe cards has successfully demonstrated that it can test die at full 125MHz array speeds," said J.S. Kih, Hynix’s director of product engineering, in a statement. "Engineering measurement of timing parameters at wafer probe correlated with that of package test well within the device margin, meaning that we can guarantee that our bare die achieve full functional specification. Ultimately, when wafer burn-in is available, package test could be completely eliminated."

Teradyne said it expects an increasing number of memory device manufacturers to move more of their testing from package to probe testing. The company estimates 70 percent to 90 percent of testing done at package is array testing, and believes these tests are candidates for a move to wafer probe. The company said this migration will be accelerated by the need to keep costs low as communication and consumer applications become dominant segments of the DRAM market.