Motorola Claims First Wafer Level Burn-in and Test Process For Flip Chips

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Motorola Inc.’s semiconductor products sector (SPS) today said it has developed and qualified the first wafer level burn-in and test (WLBT) process for flip-chip microprocessors.

Motorola aims to establish itself as a leader in providing known good die (KGD) for direct chip attach (DCA) and system-in-package (SiP) applications. WLBT was designed to allow the production of KGD for use in applications like DCA systems, multi-chip modules, SiPs, stacked-die assemblies and wafer level KGD. Motorola said industry analysts expect this emerging market to grow as much as 50 percent per year.

WLBT technology is designed to allow flip-chip microprocessors to be offered as bare-die products, with reliability equal to that of packaged devices. Previously, Motorola provided volume production of wafer level burn-in KGD primarily to the automotive industry. The company said it plans to provide the capability of combining logic, flash memory, SRAM or DRAM into a single flip-chip module or package. The intention is to use such technology on some of its future networking and communications products.

"Not only does wafer level burn-in and test offer an opportunity to experience significant cost and throughput benefits, but it is required as an enabling technology if we are going to be successful in offering module and system-in-package solutions to our customers," said Kelly Folts, product engineering and program manager with Motorola’s wireless infrastructure systems division, in a statement.

In conjunction with Tokyo Electron Ltd. (TEL) and W.L. Gore & Associates Inc., Motorola developed a wafer level test during burn-in system and full wafer direct-contact solution for bumped die used in flip-chip assembly applications. Motorola said its relationship with TEL would continue, and would produce wirebond devices and further its current KGD business in the automotive market.