Comparing ATPG and BIST

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Test challenges facing designers and manufacturers of complex semiconductor products are not new to the industry.

Increasing pressures to meet cost and time-to-market targets with innovative products while minimizing the corporate expenditures required to achieve these goals provide a daunting task.

Requirements for increased functionality and innovative differentiation continue to drive the adoption of expensive technologies and design techniques that ultimately affect the cost of the product, both in design and test.

Compounding the problem are segmented organizations in the product development supply chain and the divergent goals of these organizations. The challenge becomes how to address financial boundaries against requirements for cost-minimized differentiated products in an organizationally diverse environment.

Marketplace pressures to develop the "next big thing" at the same or lower cost than previous products have established corporate goals and mandates for both small and large development organizations.

SOC products sized at 2 million to 4 million logic gates last year are now ballooning to beyond 15 million gates, some even to 25 million gates. The design complexities involved require a review of design methods to ensure not only design success but also timely validation of product quality and integrity as impacted by the design processes.

Hierarchical plug-and-play SOC design techniques, which feature the ability to create large complex devices, must also coexist with methods that enable timely validation of the designed product. Traditional approaches for achieving timely test validation are structurally based embedded test techniques such as SCAN/ATPG.

While SCAN/ATPG has served the industry well in assisting design and manufacturing companies in testing the integrity of devices quicker than with functional test techniques, the technology is now challenged by the increase in design complexities. This challenge is represented both financially in test costs and technically with flat design methods.

New designs must consider test up-front to ensure high-integrity testing of the devices. The need for high-integrity testing requires the ability for the structural test to match design hierarchy methods and to deliver at-speed test capability. SCAN/ATPG is challenged by these requirements. Should SCAN/ATPG techniques be able to solve the challenges with design implementation, financial challenges for these new designs still remain—test time and tester cost.
By its nature SCAN/ATPG requires off-chip vector storage and control of test data. This means there are higher capital costs associated with ATE to handle the data storage and the number of SCAN channels required to minimize test time. Recently, ATPG vector storage compression techniques have been introduced to somewhat offset ATE vector storage. These techniques are challenged by their ability to handle hierarchy and ever-increasing design sizes. Furthermore, diagnostics and debug can be significantly more complicated than with conventional SCAN/ATPG.

SCAN/ATPG solutions are not reusable in environments other than semiconductor manufacturing test, which prevents large vertical multinational organizations from realizing downstream cost-savings value. For example, reuse in board manufacturing retest is not possible because of the absence of a device-level ATE to control and run the test.

Viewed from a broad business perspective, the net value/cost profile for solutions based on SCAN/ATPG will not be reflected across all organizations involved. The value will benefit only a particular segment of business and potentially do so at the expense of other organizations involved.

Corporate goals will mandate broader adoption of value across segments as these large complex design products become more prevalent. Technologies that can deliver this benefit will move to the forefront of adoption. Technology that addresses the need for timely validation and the goal of cross-organizational cost management is proven and available today. That technology is built-in self-test (BIST)-based embedded test.

BIST-based embedded test provides a structural test capability and also progresses beyond the complexity and cost limitations of SCAN/ATPG. With BIST, the test is fully contained within the device and can be controlled with a minimal amount of signals and data from ATE. BIST capability can match design hierarchy methods and fundamentally provides an at-speed test. BIST techniques are proven and available for logic, memory and some mixed signal circuitry.

Test time and ATE cost can be managed effectively with BIST approaches. The at-speed nature of BIST reduces the overall tester time and the fully contained test-set on-chip reduces the need for large data storage on ATE. These combined factors remove the trade-off of tester time and tester cost in the cost-management equation.

Value achieved at the manufacturing stage of product development transcends organizations in upstream and downstream directions. Upstream, financial and technical value is gained in the design organizations through faster implementation times and reusable test hierarchy within these large and complex designs. Downstream, the reusability of the BIST-based embedded test technology can deliver cost value to large, vertically integrated, multinational organizations in board manufacturing and application environment test.

In driving to achieve innovative, differentiated products while minimizing overall development and delivery expenditures, considerations must be made to ensure a maximum return of value. With business, “engineering” the solution often entails minimizing the instantaneous cost/value; however, minimizing the average cost/value may prove to be the best approach to deliver differentiated product value in the marketplace.