Don't let rules of thumb set decoupling-capacitor values

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Choosing decoupling-capacitor values can seem to be a "no-brainer." Unfortunately, even though the consequences of selecting the wrong values are often serious, the most commonly used methods usually produce the wrong answers.

Despite capacitors' many applications in design for electromagnetic compatibility (EMC), decoupling-capacitor values often depend on history ("This value has always worked in the past...") or on rules of thumb ("Place a 0.1-µF capacitor next to each IC..."). Although the importance of decoupling is not in dispute, designers should treat rules of thumb with skepticism and should understand the full basis for selecting decoupling capacitors. Unfortunately, some frequently used formal approaches, although mathematically sound, yield incorrect results because they fail to recognize decoupling capacitors' true role ([Ref 2](#)).

The problem with mathematical analyses of decoupling is that the models often fail to represent the real situation, so experimental work is necessary to relate theory to practice.

The results of a simple experiment help to demonstrate the concepts of decoupling. The experiment measures the magnitude of the differential ripple current that several clock oscillators generate under various loads. The experiment uses different values of surface-mount decoupling capacitors to determine the effectiveness of the capacitors as a function of both frequency and load. Three-axis
graphs (Figs 4, 5, 6, and 7) illustrate the performance differences among 470-pF to 0.1-µF capacitors.

**Importance of decoupling**

Using multilayer boards that have planes dedicated to V_{CC} and ground enhances the operation of decoupling capacitors in two major ways. First, power planes decrease the inductance between capacitors and ICs. Second, power planes give all ICs on a board a high-quality (that is, low-inductance), high-frequency distributed capacitance. (For planes separated by 0.006-in.-thick FR-4 material, the capacitance is roughly 150 pF/in².) Apparently as a result of severe cost pressures throughout the industry, manufacturers are using a surprisingly large number of two-layer boards. Proper decoupling of ICs is mandatory to control differential-mode (DM) radiation from two-layer boards (Refs 1 and 2).

Although shielding is sometimes an option for containing electromagnetic radiation from pc boards, shielding is often impractical, because it involves metal plates. Metals, even when passivated, cannot withstand some of the harsh, corrosive environments in commercial applications. This situation necessitates noise control on the board. With a two-layer board in a plastic enclosure, proper decoupling can greatly affect DM radiation. The difference that decoupling produces in radiation can spell the difference between a product's passing or failing regulatory-agency tests of RF emissions. In most cases, government or commercial rules prevent companies from selling products that fail such tests.

Another reason to control noise before it leaves the pc board is cost reduction. If noise radiates from a pc board, you can enclose the board in a metal box. Such shielding often proves inadequate, though. The next step is to add some combination of filters and gaskets. Such measures are expensive. A dollar's worth of pc-board-mounted components along with a judicious board layout can work better than $20 worth of filters, gaskets, and shields.

Yet another reason for controlling noise emissions from pc boards relates to noise immunity. If you contain emissions from your product, the product almost always becomes less susceptible to interference. Measures to reduce radiation from pc boards usually also reduce your product's susceptibility to radiated and conducted noise. In most cases, these measures are far less expensive than retrofits aimed solely at obtaining agency approvals by reducing susceptibility.

However, one of the most important reasons for proper IC decoupling has nothing to do with meeting federal or international standards: Proper decoupling makes a product more reliable. For example, consider a scenario in which multiple boards plug into a backplane. If the plug-in boards ignore or improperly implement decoupling, a significant amount of voltage ripple appears on the backplane and degrades system performance. Boards that contain high-power devices can adversely affect other boards that share the same bus. For example, boards that don't tolerate overvoltage or undervoltage conditions—even short-duration conditions—can malfunction as a result of improper decoupling on other boards.)

As IC technology continues to advance, chips require more power more quickly. This requirement demands proper decoupling. Proper decoupling involves multiple approaches: distributed capacitance between the V_{CC} and ground planes for very high frequencies (this method works only on multilayer boards), localized chip decoupling for high frequencies, and bulk decoupling on each board for lower frequencies and higher power. Choosing local decoupling capacitors for individual ICs is a concern only with the second approach.
The nonideal capacitor

The traditional concept behind using capacitors to decouple ICs is to give each IC a localized reservoir of high-frequency energy. The bulk decoupling capacitor on the circuit board or the power supply's output capacitor, in turn, replenishes the local capacitor by furnishing a lower amplitude, longer duration current. In essence, the local capacitor helps to "decouple" the IC from the main $V_{CC}$, decreasing the magnitude of the high-frequency ripple or sag that appears on the main power bus.

Unfortunately, a capacitor is not an ideal element; rather, you can model it as a series LCR circuit (Fig 1). C is simply the value of the capacitor itself. L and R are parasitic elements that limit the capacitor's performance. When you place a capacitor on a board, the additional inductance of the traces and the chip leads further degrades the component's performance.

Because the nonideal capacitor consists mainly of reactive components, its response varies as a function of frequency. If you "drive" the circuit of Fig 1 with a swept-frequency ac source, you can use PSpice, Microcap, or another circuit-analysis program to calculate this response. You can also measure the response with an impedance analyzer. This measurement is not as easy as it might seem, however, because the inductance of the measuring probe can make the capacitor look worse than it actually is.

Ref 3 analytically derives the impedance of a capacitor. The net impedance of the series-LCR circuit is the sum of all of the circuit elements' impedances. Thus, at low frequencies, the capacitive reactance is very high, becoming an open circuit at dc, and dominates the impedance. As the frequency increases, the capacitive reactance decreases at a rate of 20 dB/decade, whereas the inductive reactance increases by 20 dB/decade. The capacitive reactance dominates the capacitor's net impedance up to the self-resonant frequency (SRF), $1/\sqrt{LC}$. At this frequency, the capacitive and inductive reactances are equal but opposite in phase, and the impedance is simply the equivalent series resistance. Above the SRF, the impedance begins to increase, as the inductive reactance now dominates (Fig 2). At frequencies much higher than the SRF, you might incorrectly infer that the capacitor is ineffective for decoupling.

Although the value of the capacitor is fixed, the inductance depends on the capacitor's type and how you mount the component on the board. The primary sources of inductance include capacitor lead length, trace length, and IC lead length. Common methods for reducing the net inductance are: using leadless chip capacitors, shortening or widening traces to the chip, using inherently lower inductance IC packages (such as SOIC or QSOP), and mounting the capacitor on the side of the board opposite the IC. The last method, although effective in some applications, significantly increases the board's fabrication cost.

The traditional approach for sizing a decoupling capacitor is the simple relationship shown in Eq 1.

\[ i = C \frac{dv}{dt} \quad (Eq \ 1) \]

You can simplify this to the classic Eq 2.

\[ C = \frac{it}{V}, \quad (Eq \ 2) \]

where $C$=needed capacitance, $i$=output current, $t$=rise time of output, and $V$=voltage ripple on the bus. This relationship indicates that the faster the logic family, the smaller the required decoupling capacitance. Also, devices that supply higher output current require more capacitance. Because the energy stored in a capacitor is $C \times V^2/2$, lowering the noise on the voltage bus requires that you
increase the capacitance.

Prominent among these harmonic-frequency sine waves are those associated with the waveform period, the durations of the waveform's positive and negative portions, and the waveform's rise and fall times. All of these frequencies show up in the ripple on the bus. **Eq 2** addresses only the rise time.

As an example, calculate the decoupling required for a 33-MHz clock that has an output rise time of 2 to 3 nsec. The clock supplies a current of no more than 10 mA. If the desired supply-voltage ripple is 50 mV, the classical method yields the following value of decoupling:

\[
C = \frac{it}{V} = \frac{(10 \text{ mA})(2 \text{ nsec})}{50 \text{ mV}} = 400 \times 10^{-12} \text{F} \approx 400 \text{ pF}.
\]

A designer knowing no more than **Eqs 1** and 2 would incorrectly assume that a 470-pF decoupling capacitor would be adequate and would perhaps use 1000 pF to be safe. According to this method, a value of 0.1 µF or even 0.01 µF is clearly overkill. Moreover, larger value capacitors are supposed to be ineffective for decoupling because they self-resonate at relatively low frequencies (0.1 µF self-resonates below 5 MHz, and 0.01 µF self-resonates below 15 MHz).

The circuit used in the experiment appears in **Fig 3**; however, the experiment varies the following parameters:

- **clock frequency**: 33, 50, 66, and 100 MHz
- **output load**: 10 k Ohm, 10 k Ohm in parallel with 10 pF, 10 k Ohm in parallel with 100 pF
- **decoupling capacitance**: none, 470 pF, 1000 pF, 4700 pF, 0.01 µF, 0.022 µF, 0.047 µF, 0.1 µF.

A distinct advantage of the experiment (**Fig 3**) is that it does not require a special test facility, such as an anechoic chamber, but can be performed on a benchtop at an EMC-integrity lab. The decoupling capacitor, C, is always a leadless chip capacitor—the only type of capacitor in the experiment. The oscillator that imposes transient loads on the power supply provides a practical demonstration of the benefits of proper decoupling. Most equipment that must meet EMC requirements includes circuits that have similar decoupling requirements. The oscillator delivers a quasi-square wave to its load and draws high-frequency current from the power-supply bus. In the experiment, the oscillator output connects to a light load, a standard load that simulates one gate, and a heavy load equivalent to many gates. Because of the power-supply bus's inherent impedance, the oscillator's supply current generates voltage ripple on the bus that can interfere with the correct operation of other devices or can cause DM radiation.

The oscillator mounts on a small, single-layer pc board, and copper tape simulates a multilayer board's V \text{cc} and ground planes. Therefore, leadless chip capacitors work effectively without leads. Leads would greatly degrade the capacitors' performance. The experiment uses Fox 33- and 50-MHz oscillators and Saronix 66- and 100-MHz oscillators. The circuits draw power from a 5V-dc supply via approximately 2.5 ft of twisted-pair wire, which simulates the source impedance that might drive the oscillator in a typical application. The circuit load connects directly across the output to minimize the loop area. Thus, coupling to the V \text{cc}/ground loop is minimal. A current probe placed differentially around the V \text{cc} and return lines mitigated the effects of common-mode currents. Such currents could confound these measurements.
Experimental results

These experiments aim to resolve some uncertainties relating to capacitor-value selection. One of electrical and EMC designers' prime functions is to select the correct capacitor for each IC. Many engineers resort to rules of thumb or "gut-feel" to determine values.

Decoupling-capacitor selection should be more scientific but must address several variables. Exactly how should you vary the capacitor value as you vary the clock frequency? Does clock loading affect the capacitor value? The experiment attempts to show how the capacitor affects the power-supply distribution in a real circuit—not a mathematical model.

In reviewing the results, use the amplitude values as figures of merit only. Although decreasing the DM current decreases the far-field radiation, the experiment makes no attempt to establish this correlation.

Although the 3-D representations of the data that appear in Figs 4 through 7 show some fascinating phenomena, remember that the experiments use relative measurements. All of the measurements use the same current probe in the same test setup. The DM current measurements are in "raw" units of decibels referred to 1 µV. To convert the data to decibels referred to 1 µA, subtract the transfer impedance of the current probe (Tegam MN 94111-1), which is nominally 14 dB Ohm (roughly 5 Ohm).

Although the probe works up to 1 GHz, the amplitude of the harmonics of the fastest clock fell below the test setup's noise floor at higher frequencies. Thus, the experiment provides limited data above about 600 MHz. Finally, because the current probe is placed differentially around the lines to reject common-mode currents, the actual differential current from the oscillator is 6 dB less than the figures show. Moreover, although the experiment does not consider common-mode currents, do not conclude that common-mode currents are unimportant. Rather, common-mode effects are simply outside the scope of the experiment.

Surprising results

The results of these experiments are both surprising and interesting, because they refute some common thinking about the effectiveness of decoupling capacitors at high frequencies. Figs 4 through 7 show the graphs that most dramatically illustrate the experiment's important points.

One of the most surprising results is that 470 pF provides no decoupling at any frequency under any load. See Fig 4, in which the 100-MHz oscillator drives its lightest load, a 10-k Ohm resistor. In this graph, you can see that the current ripple with no decoupling is practically identical to the current ripple with a 470-pF decoupling capacitor. This means the capacitor provides no energy to the clock; all energy comes directly from the power supply via the twisted pair.

Although this result may seem counterintuitive, consider the impedance of the capacitor vs the impedance of the twisted pair and the ability of each to supply energy. The characteristic impedance of the twisted pair is about 120 Ohm. The impedance of the 470-pF capacitor must be less than 120 Ohm if the capacitor is to supply energy to the oscillator. Conversely, the greater the impedance of the 470-pF capacitor, the less energy the capacitor supplies. The data indicate that at all frequencies of interest, 470 pF simply acts as too high an impedance to provide any decoupling. The poor performance of the 470-pF capacitor would be even more pronounced with a multilayer board. In such a board, the impedance of the Vcc and ground planes is on the order of tens of ohms.
Even a cursory examination of Figs 5 through 7 reveals several things. First, the lack of a decoupling capacitor increases the differential-mode emissions on the power cable by approximately 20 dB. The effectiveness of the decoupling capacitor appears to deteriorate at speed higher than about 500 MHz. The capacitor's effectiveness does not really deteriorate, however. Further investigation of this effect shows that, without decoupling, the rise time of the output waveform is 2 to 3 nsec. With a 0.01-µF decoupling capacitor, the rise time decreases, suggesting that, because the decoupling capacitor is a better source of high-frequency energy, the oscillator can drive its output faster. This phenomenon is also evident in Fig 4.

**Watch out for common-mode radiation**

The implications of these findings are both good and bad. If timing and clock skew are critical, proper decoupling can help by decreasing the rise time of output waveforms. The bad side is that these output signals (clocks, data, and address lines, for example) determine the common-mode (CM) interference from the board. Other techniques effectively and inexpensively control CM emissions. In other words, you can improve the reliability of a design by carefully selecting decoupling capacitors, but you must be on guard, lest the measures you take to reduce DM radiation degrade other aspects of the board's performance.

Next, it is clear that, over the investigated frequency range, almost any value of decoupling capacitor dramatically reduces DM emissions. The contribution of decoupling capacitors over such a wide frequency spectrum is an important and surprising result. Current wisdom in EMC design is that capacitors of 0.01 µF and larger provide little or no decoupling above 15 MHz. This belief results from a graphical interpretation of capacitor frequency response and self-resonant frequency. The measured data show that, on the contrary, such capacitors are effective over a wide frequency range in reducing the DM emissions that appear on the power cord. In almost all cases, however, the frequency response seems to improve with capacitance values smaller than 0.1 µF; the old standby 0.1-µF capacitor, then, has had its day. Though it does not provide as much improvement as expected, a 0.01-µF capacitor performs better overall than a 0.1-µF part.

The optimal value of decoupling capacitance does not depend on the load the oscillator drives. A comparison of Figs 5 through 7 (light to heavy load) shows that, as the baseline emissions increase, so do the "decoupled" emissions. That is, under very light to very heavy loads, 4.7-nF to 0.1-µF capacitors supply enough energy to the oscillator to provide the same decoupling. The 1000-pF capacitor has little effect on the fundamental frequency, although it reduces the harmonics about as well as the other capacitors. This fact indicates that, for the lower frequencies, 1000 pF acts as too high an impedance to effectively supply energy to the IC. We call this effect the "470-pF syndrome."

**Conclusions**

So, what is the optimum capacitance for a given application? Some immediate conclusions are that a 0.1-µF capacitor is not the optimum value. You should also avoid "small" values of decoupling, particularly 470 and 1000 pF. The data indicate that such small capacitors do not reduce noise on power-supply buses as well as higher value capacitors do.

In the example, the equation CV=it yields a capacitance of ~400 pF. This value is inadequate because it decouples only the harmonics associated with the waveform edges. The small decoupling capacitor neglects the fundamental frequency, the frequencies related to the pulse width, and the
harmonics of these frequencies. The equation provides only a lower boundary for decoupling capacitance. Contrary to what many EMC texts say, do not use this equation to calculate decoupling-capacitor values.

All values of capacitors from 4.7 nF to 0.1 µF provide fairly comparable decoupling. A careful examination of the test data, however, shows that a 0.01-µF capacitor provides the best overall IC decoupling.

Authors' biographies

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References