Mentor: Making Design Reuse Work

Jeff Jussel - December 06, 1999

Despite all the recent hype, design reuse is not new. Engineers have been practicing reuse since the Unix copy command was first implemented.

But much more planning is required to achieve global design sharing. Large-scale productivity gains from reuse come only from deliberate and calculated investments in design infrastructure. For reuse to be successful, a comprehensive design reuse infrastructure must support a block-based system-on-a-chip (SOC) methodology.

The value of design reuse is clear and engineers are rising to the challenge with larger, more complex SOC devices. According to an industry report, designers expect their average chip size to grow by 39 percent next year, trending to more than 500,000 gates. Many organizations already routinely generate SOC designs of over 1 million gates. With development schedules staying constant, design reuse is an SOC productivity requirement.

In this situation, designers are building on their own and their colleagues' previous work by reusing design components. In fact, a recent survey reports that 70 percent of chip designers expect to work on SOC projects involving some reusable components within a year. Across the industry, over half of the design engineers are working on the development of reusable intellectual property (IP). These activities cover a spectrum of reuse from third-party IP blocks intended for general release to internal SOC elements that will only be reused locally.

Reuse Still a Challenge

But the trend towards reuse is far from universal. A sizable group of engineers plan no reuse at all, citing technical difficulties, legal hassles and a preference to work completely in-house. In fact, there are significant barriers to increasing SOC productivity through design reuse.

Typically it is the technical problems that are the most apparent. Despite the work of industry associations and corporate initiatives, there are still few standards that can be applied universally. Even within companies, designers attempting reuse will find incompatible deliverable formats,
mismatched block interfaces, incomplete documentation and inconsistent tool flows. In many cases, there is no clear definition of what it means for a block to be reusable. To further complicate matters, the definition of "reusable" differs between designers, organizations and design requirements.

With growing chip complexity, functional verification is also a formidable barrier to design reuse. If a designer must be intimately familiar with the minutiae of a component in order to verify that block, then little time is saved in design reuse. Verification is estimated to take up 60 percent or more of the typical design schedule, so reuse of functional verification may be the most important element for improving design productivity.

Going beyond the technical issues, there are other daunting barriers to the adoption of a design reuse methodology. Road maps must be determined to identify what IP will be reused. While some of this IP can be purchased externally, the majority of reusable design blocks will be extracted from existing internal stores of design data.

A defined make vs. buy decision process must include a myriad of issues, including cost, state of existing data, legal contracts, the target design schedule and even the availability of engineering resources. Few organizations have the resources required to re-engineer all legacy design elements in order to make them reusable.

On top of all this, your company must find ways to encourage design engineers to choose design reuse. The adoption of reuse as a standard part of the engineering culture may be the most difficult problem of all.

The Infrastructure

A well-planned design reuse infrastructure addresses these barriers. Design data submitted for reuse is checked subjectively against required technical standards. The database is capable of storing and preserving design data in an accessible manner. The system also serves as a means of communication between designers. And ultimately the design reuse environment supports the productivity of the SOC designer. The industry is beginning to recognize this need. In a recent survey, 32 percent of companies declared they either had, or were working on, some form of IP repository. More telling for the future of design reuse, 89 percent of those companies expected the role of the IP repository to grow as part of the SOC design environment.

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Reuse environments span a spectrum of increasing customization from low- to high-level design reuse. The basic mission of these IP repositories is to control and protect the reusable design data. A typical low-level design reuse repository consists of a relational database made up of metadata, or non-design information about the IP. Actual design data is then included with an appropriate revision control system. Global SOC design teams collaborate more easily with the aide of a suitable configuration and project management system.

Beyond data protection and delivery, the goal of the IP repository is communication between
designers. To maximize ease of communications, the IP repositories are often Web-based, allowing the search, select and download capabilities familiar to that medium. Designers are made aware of the status of IP on the system through means of IP qualification levels. And with such a system, design updates and bug alerts can be sent via e-mail to every designer using a particular component.

To ensure the productivity gains of design reuse, features such as automated SOC integration and verification can be added to create a high-level design reuse infrastructure. The automated features of a high-level system require a chip specification to be entered as design metadata to communicate implementation details to a tool-independent flow management system. With this information, the IP design environment can connect hard or soft components and automate the manipulation of design data through tape-out. Tool-scripts can be parameterized and included as data in the repository.

High-level reuse environments also address functional verification, the hardest SOC productivity problem. In these systems, functional test suites are reused with design flow automation. While high-level reuse environments require more customization, they also provide the most productivity and reduce the amount of IP re-engineering needed for reuse.

**Reusing the Infrastructure**

The customized nature of a complete reuse environment implies that design reuse infrastructures must be unique for each design organization. Fortunately, there are ways to "reuse" elements of the design infrastructure.

At Mentor Graphics, we use a core set of software, methodology and algorithms, called the QuickUse Development System (QDS), to implement global low-, mid-, and high-level design reuse infrastructures for major system and semiconductor companies. Like most reuse systems, QDS provides a Web-based repository of design data. However, the QDS environment also supports the subjective qualification and IP data and automates the integration and verification of SOC designs through the reuse of those cores. The SOC design flows supported by the QDS system are electronic design automation (EDA) vendor-independent for maximum flexibility. The QDS environment is also based on open industry standards like Java and Oracle to remain expansible and customizable.

Since the implementation of a reuse environment is a highly customized process requiring knowledge of SOC design processes, Mentor delivers this infrastructure through its consulting organization, where I work. Building on the experience of promoting design reuse internally and in customer environments, Mentor Consulting employs a systematic approach. The process begins by developing a complete understanding of the technical and business issues facing the design organization. Next, a comprehensive solution is planned that addresses the issues and augments the strengths of the organization through design reuse. A customized infrastructure is then implemented and tested against a proof-of-concept SOC design project.

Whether it is primarily a data repository or a completely automated reuse engine, the design reuse infrastructure needs to remove the major reuse barriers to reuse to enable SOC productivity gains. With that goal in mind, reuse environments can be expanded far beyond a copy-modify reuse solution.

Current reuse environments, like QDS, can automate certain integration and verification features. In upcoming solutions, the scope of verification will be expanded to include firmware and application software that runs in existing co-verification tools. Reusable software elements can serve as functional verification test suites for the hardware. System verification will be made more complete by providing easier access to rapid prototypes through the reuse of hardware and software components.
Well-planned design environments can ensure the successful introduction of design reuse across an organization. And future advances will open the way for the routine development of multimillion gate SOC devices. However, just as designers must now choose the proper tool flows, reuse infrastructures will always need to be customized to the needs of the user. The success of design reuse is measured by the productivity gains of the SOC designer.

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