The Design Team Culture for IP Reuse

Adriaan Ligtenberg - January 31, 2000

The System-On-Chip revolution is upon us. There is little doubt that the leading high-tech companies of today are in danger of being left in the dust of history if they cannot successfully transition to SOC design, and quickly.

Adriaan Ligtenberg is senior vice president of Methodology Services at Cadence in San Jose. He is native of Amsterdam, The Netherlands, and worked before Cadence at Bell Labs, among other places.

The reasons for this shift are becoming well-known: semiconductor manufacturing advances have provided us with millions of transistors on a single die, and designers taking advantage of this under-developed silicon "real estate" must learn to reuse existing intellectual property. Creating every circuit from scratch is no longer practical in these times of lightning-quick product cycles driven by competition and insatiable market demand for the latest feature-laden products.

What is less well-known is how to make the SOC transition. There is an existing culture within semiconductor design teams that inhibits IP reuse. Chips are designed, built, and shipped with little regard for how this valuable IP can be re-engineered to create new products.

One need look no further than the structure of large semiconductor houses to realize the truth in this. Most are organized into distinct divisions by application area, with one group specializing in communications, another in processors, a third in memory, and so on. ASIC teams within systems companies deal with the same complexities. While all share the common goal of overall corporate betterment, each is typically judged by its individual productivity -- there is no incentive for cooperation or even basic communication between the groups.

Breaking down these barriers is a daunting task, but one that must be undertaken swiftly if a company truly hopes to be a player in the SOC game.

A good starting point is incentives. Draw engineers into the process, make them see the value in

designing blocks for ready reuse, and invent a system of rewards. For instance, when designers come up with elegant solutions that have widespread reuse potential, these efforts should be recognized and rewarded.

Next are the technical aspects of IP reuse. First, provide a clear set of IP authoring guidelines that build consistency across the entire company, letting all designers create blocks that can be quickly integrated with others authored under the same guidelines.

Cadence recently helped Japan's Oki Electric develop such guidelines that serve as a model for this type of document, covering such issues as naming, clocking and test practices, coding, documentation, and model packaging. Clear documentation lets other designers quickly understand the functions of the block and its suitability for a given application.

Access to the reusable IP offers the next challenge, but corporate Intranets provide a ready answer. The huge amounts of data contained in these libraries -- usage history, reference implementations, RTL files, synthesis scripts, timing models, netlists, and much more -- make them unwieldy for any storage solution that is not Web-based.

In addition, an interesting thing is happening on the way to SOC. Many companies are fitting IP into platform-based SOC designs targeting specific applications, like digital cameras. The benefits are focused product development and rapid derivatization -- natural, yet unexpected benefits flowing from the simple idea of designing for reuse.

With the advent of SOC we are once again witnessing one of those happy convergences of markets and science that have traditionally driven the electronics industry to new heights of progress and profitability. With proper planning, foresight, and leadership to ensure design reuse, any company wishing to take full advantage of the opportunity presented by SOC can achieve success.

Adriaan Ligtenberg is senior vice president of Methodology Services at Cadence in San Jose. He is native of Amsterdam, The Netherlands, and worked before Cadence at Bell Labs, among other places.