Synchronize asynchronous reset

Willy Tjanaka - January 06, 2000

Synchronous reset and asynchronous reset are both common reset mechanisms for state machines, and the reset circuit in Figure 1 combines the advantages of each. Synchronous reset has the advantage of synchronization between clock and reset signals, which prevents race conditions from occurring between the clock and the reset signal. However, synchronous reset does not allow a state machine to operate down to a dc clock because reset does not occur until a clock event occurs. In the meantime, uninitialized I/O ports can experience severe signal contention.

Asynchronous reset has the advantage of allowing state machines to operate down to dc clock. This operation is possible because asynchronous reset immediately initializes the state machine when a reset signal occurs independently of the clock. Unfortunately, asynchronous reset may cause a race condition between the reset signal and the clock. Race conditions can cause problems, including metastability or wrong-state initialization.

The reset circuit in Figure 1 asserts the reset signal immediately after detecting the asynchronous reset signal. However, the circuit also synchronizes the reset release with the clock. The circuit uses this synchronized asynchronous-reset signal to drive a state machine that uses flip-flops and the asynchronous-reset input.

The reset circuit consists of two back-to-back D flip-flops that synchronize the asynchronous reset signal. In addition, the asynchronous reset causes the D flip-flop outputs to immediately go low. Figure 1 also shows the corresponding signal names for the Verilog description of the circuit (Listing 1), which you can immediately incorporate into a design or simulation. Figure 2 shows the simulation waveform from the Verilog code in Listing 1 using Altera Max+PlusII. Observe that the circuit immediately asserts the output-reset signal (orsr_n) when the system asserts the input reset signal, irst_n. Also notice that the reset release is synchronous with the clock within two cycles. (DI #2465)