Analog Devices SHARC DSP

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The 32-bit fixed- and floating-point SHARC DSPs, or ADSP-2106x and the second-generation ADSP-2116x, integrate four internal buses, a large on-chip memory, and an I/O controller to offload I/O. Both single-instruction-multiple-data (SIMD) and single-instruction-single-data (SISD) versions are available. Within the SISD CPU core, the ALU, multiplier, and shifter operate in parallel to perform multifunction, single-cycle instructions. The SIMD core adds a second compute block that includes an additional parallel ALU, a multiplier, a shifter, and a register file. This arrangement allows both computation blocks to process the same instruction but operating on different data.

SHARC DSPs feature an enhanced Harvard architecture in which the data-memory bus transfers data and the program-memory bus transfers both instructions and data. With its separate program- and data-memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction from cache in one cycle. The 32-entry, 48-bit-wide instruction cache is selective—caching only the instructions whose fetches conflict with accesses to program-memory data.

The SHARC DSP uses a general-purpose, 10-port, 32-register data-register file to transfer data between the computation units and the data buses and to store intermediate results; the ADSP-21160 duplicates this action. The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-2106x DSPs can conditionally execute a multiply, an add, a subtract, and a branch in one instruction.

SHARC DSPs feature two data-address generators (DAGs), which implement circular data buffers. These DAGs contain sufficient registers to allow you to create as many as 16 primary and 16 secondary circular buffers. The DAGs, which may start and end at any memory location, automatically handle address-pointer wraparound.

SHARC chips have two high-speed serial ports and a host/parallel port, providing a direct interface to off-chip memory, peripherals, and a host processor. Link ports facilitate interprocessor communication and bus arbitration among as many as six ADSP-2106x chips.

The SHARC's CPU executes using on- or off-chip memory. Some SHARC chips contain as much as 512 kbytes of on-chip memory organized into two banks of dual-port RAM. You can use this memory to store a combination of 16-, 32-, or 40-bit data and 48-bit instructions and perform as many as four accesses per cycle: program memory for code and data, data memory for data, and an off-chip load using the chip's I/O controller.

SHARC's I/O controller executes I/O transfers in parallel with CPU execution. The I/O controller offloads reads and writes between on- and off-chip memory. The dual-ported, dual-banked nature of the memory, combined with the I/O processor, allows the core and the DMA to simultaneously access internal SRAM. The I/O controller manages all DMA channels, transferring data among
internal and external memory and all peripherals, such as the host port, as many as eight serial ports, and six link ports. All DMA operations generally do not interrupt or delay core thread execution. The DMA controller allows you to dynamically control the external-memory-bus width. The synchronous serial ports support time-division-multiplexed serial streams and hardware companding and can transfer data as fast as 40 Mbps. In all but the ADSP-21065L, the six communication ports move data in 4-bit nibbles, transferring as much as 1 byte/clock cycle. With six links operating simultaneously, maximum throughput is 600 Mbytes/sec.

The CPU, I/O controller, and peripherals interconnect and perform flexible, nonintrusive transfers through a multibus-crossbar-interconnection unit. To reduce bottlenecks, the interconnect crossbar permits unlimited data and instruction movement from external or internal memory or cache and permits I/O from on- or off-chip peripherals—all in one cycle.

The 211660, 21060, and 21062 provide six communication ports for array multiprocessing. These ports feed through the I/O controller and let you create meshes of DSPs that can access each other’s memory spaces. (Point-to-point connections between DSP ports define each processor in the mesh.) The on-chip I/O controller sets up, runs, and responds to these ports. Transfers pass through the I/O ports to and from internal memory. The I/O controller separates these transfers from mainstream DSP.

A parallel port serves as a direct interface to off-chip memory, peripherals, or a host processor. As many as six SHARCs can share this interface with a host processor. SHARCs offer a unified address space using a 32-bit address bus and a 32- or 48-bit data bus. For a 100-MHz clock, the chip supports a 10-nsec access time with zero-wait-state memory. The special host interface supports both 16- and 32-bit µPs, as well as system buses, such as ISA and PCI. The host treats the SHARC as a memory-mapped device with direct writes or reads to internal memory.

The lowest priced SHARC DSP, the ADSP-21065, also provides a synchronous DRAM (SDRAM) interface that transfers data to and from SDRAM as fast as 240 Mbytes/sec, or twice the clock frequency. The glueless SDRAM interface can access 16- or 64-Mbyte SDRAMs and enables you to connect to any one of four external memory banks.

**Addressing modes**—SHARC offers immediate, indexed, bit-reversed, circular-modulo, and register-direct and -indirect addressing. (It must use indirect addressing for off-chip memory access.)

**Special instructions**—SHARC provides bit manipulation, division iteration, reciprocal of square-root seed, conditional subroutine call, single and block repeat with zero-overhead looping, fixed- and floating-point compare, and conditional execution of most instructions. SHARC supports IEEE-754 single-precision, floating-point (23-bit data, 8-bit exponent, and sign bit), and a 40-bit extended IEEE format for additional accuracy (32-bit data).

**Support**—Analog Devices’ software- and hardware-development tools include the company’s VisualDSP integrated development environment, in-circuit emulators, and a development kit. VisualDSP provides the interface to an optimizing C compiler, an assembler, a linker, a simulator, and a debugger. Analog Devices’ emulators are available for Universal Serial Bus, PCI, and Ethernet host platforms. An EZ-Kit Lite consists of an evaluation board and limited but full-featured VisualDSP. Analog Devices based the SHARC assembly language on an algebraic syntax.