Atrenta announces SpyGlass-Physical; ST cites success

Suzanne Deffree - June 17, 2010

ANAHEIM, CA. -- Atrenta at the Design Automation Conference (DAC) announced the availability of its new SpyGlass-Physical product. The new addition to the SpyGlass family enables RTL (register transfer level) engineers to achieve faster design closure by modeling physical implementation effects at the RTL stage of the design. Previous members of the SpyGlass family provide information on whether a design is syntactically correct and testable; the new member provides early estimates of area, power, timing, and routability for RTL designers who lack physical design expertise or tools.

Ravi Varadarajan, Atrenta fellow, said the new tool does not replace a customer's favorite implementation tools but rather makes the existing tools more efficient, allowing designers to identify problems earlier in design cycle. In addition, the time penalties involved in successive iterations using traditional tools (in which you find problems after place-and-route, for instance) limit the amount of exploration designers can do, with the result that they might settle for a suboptimum solution. SpyGlass-Physical, Varadarajan said, alleviates that problem.

François Rémond, director of CAD at STMicroelectronics, described his use of the SpyGlass-Physical tool in the design of a 55-nm set-top-box chip, which includes 209 million transistors, 230 clocks, 7 million placed instances, 500 signal pads, 53 RTL IP blocks, and 160 hard IP blocks. He explained that the timing and physical closure of such chips represents a big challenge.

"We needed a tool that would partition our SOCs based on our requirements, and provide trade-off analysis and guidance for our implementation tools. The SpyGlass-Physical product was able to achieve just that on 40-nm and 32-nm SOCs in significantly shorter time than we expected," Rémond said.

He said he has experienced SpyGlass-Physical runtimes in the range of two to three hours, which represents a significant savings over finding problems deep down into the implementation process.

The product helps to achieve performance targets in concurrent block/SOC development processes by using a set of interactive implementation analysis features. The result is enhanced guidance for the actual implementation of both IP blocks and full-chip SOCs. Existing SpyGlass users can easily integrate the product into their design flow and realize the benefits of early physical implementation modeling.

"Chip design companies have a great need to reach faster design closure than what is supported by current flows," said Dr Ajoy Bose, chairman, president, and CEO of Atrenta. "The ability to model the impact of physical implementation on the design at an early stage is a critical aspect that is missing from today's RTL flows. The SpyGlass-Physical product addresses this gap by providing early estimates of area, power, timing, and routing congestion."