Architecture combines low- and zero-IF receivers

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Low-IF (intermediate frequency)-receiver architectures are increasingly popular for many wireless standards. You can detect the signal at the IF or downconvert it to baseband after the ADC stage. This circuit does the final downconversion using a switch-matrix mixer before the analog-to-digital conversion. You use analog filters following the mixer stage. This approach reduces the dynamic range the following ADC stage requires. By doing simulations and taking measurements on a prototype, you can investigate the effect of nonideal switches in the matrix.

Before delving into the details, you should understand the history of this architecture. The superheterodyne receiver has for decades been the architecture of choice because it provides excellent receiver properties, such as selectivity and sensitivity. The architecture does not easily lend itself to integration, however, because you must implement the image-rejection filters in a discrete circuit.

Direct-conversion, or zero-IF, receivers have recently gained importance (Reference 1). This architecture is appropriate for integration, but it causes other problems. A direct-conversion architecture has dc-offset problems that necessitate a dc-nulling strategy (references 2 and 3). In body-worn radio equipment, the antenna’s impedance matching changes frequently. In this case, it is difficult to build a wellbehaved dc-nulling circuit. Furthermore, modern high-speed modulation schemes must have a continuous baseband spectrum without gaps.

To avoid this problem, you can build low-IF, or quasi-direct-conversion, receivers (Reference 2). The desired signal bandwidth after a low-IF-conversion step is on either the positive- or the negative-frequency side, but it does not include any dc part of the spectrum. You can then ac-couple the subsequent ADC.

The final downconversion to baseband usually takes place in the digital domain. You multiply the complex signal with a rotating phasor. Choosing a low IF that is one-quarter of the sampling frequency eases these operations by reducing the number of multiplications to those for swapping samples and changing their signs every other time.
To illustrate this approach, you denote the incoming signal at low IF as \(s(t)\) and mix down the signal with frequency \(f_{\text{LO}}\) (Equation 1):

\[
\bar{s}(t) = s(t)e^{-j2\pi f_{\text{LO}} t}.
\]  

(Equation 1)

You then sample Equation 1 with a sampling frequency \(f_s\) of \(1/T_s\):

\[
\bar{x}(t) = \sum_{k=-\infty}^{\infty} s(kT_s)e^{-j2\pi f_{\text{LO}} kT_s}.
\]  

(Equation 2)

You choose \(f_{\text{LO}}\) to satisfy Equation 3:

\[
f_{\text{LO}} = \frac{f_s}{4} = \frac{1}{4T_s}.
\]  

(Equation 3)

Equation 2 then results in Equation 4:

\[
\bar{x}(t) = \sum_{k=-\infty}^{\infty} s(kT_s)e^{-j\frac{\pi}{2} k} \\
= \sum_{k=-\infty}^{\infty} s(4kT_s) - j \sum_{k=-\infty}^{\infty} s((4k+1)T_s) \\
- \sum_{k=-\infty}^{\infty} s((4k+2)T_s) + j \sum_{k=-\infty}^{\infty} s((4k+3)T_s).
\]  

(Equation 4)

If you represent signal \(s(t)\) in its I/Q (inphase/quadrature) form as a real and an imaginary part, you can rewrite Equation 4 as Equation 5:
This form represents the switching function. The major drawback of this technique is if only real analog filters are applied before the analog-to-digital conversion, the ADCs must have a high dynamic range. Wireless-communication equipment has adjacent-channel rejection on the order of 70 dB. In this case, the adjacent channel is the image frequency corresponding to the negative frequency of the desired signal. The ADC must provide more than 12 bits of dynamic range, including the possible signal dynamics of nonconstant envelope-modulation schemes. These ADCs are expensive, and they consume a lot of power.

A possible approach is to apply polyphase filters, which can separately filter the negative and positive frequencies (Reference 4). This approach increases the circuit’s complexity for a given order of filters because the coefficients of such filters are both real and imaginary.

Downconverting the signal from low IF to zero IF before filtering and analog-to-digital conversion eliminates the need for polyphase filters and still uses an ADC with reduced dynamic range.

### Architecture and circuit

You can use switches as mixers in downconversion architectures by assuming that you have both the inverse and the noninverse of the real and imaginary parts of the signal (Reference 5). The switch-matrix mixer comprises eight switches operating in four phases that feed the four signals, I+, I−, Q+, and Q−, to the input of a subsequent filter. You can implement the matrix with transmission-gate FET switches. The equivalent operation of these switches is mixing by one-fourth of the sampling frequency (Equation 6):

\[
f_{\text{LO}} = \frac{f_s}{4}. \tag{5}\]

You insert the switch matrix into the receiver chain (Figure 1). The numbers assigned to the switches denote the phases when they are closed. You drive the switches with phase-shifted signals (Figure 2). The switching function, G(t), applies the mixing process to signal s(t) (Equation 7):

\[
\tilde{x}(t) = \sum_{k=-\infty}^{\infty} \left[ \text{Re}(s((4k+3)T_s)) + j \sum_{k=-\infty}^{\infty} \text{Im}(s((4k+3)T_s)) \right]. \tag{6}\]
\[ \hat{s}(t) = s(t) \times G(t). \]  

The switching function, \( G(t) \), has some harmonics, requiring you to apply some filtering after the mixing process (see sidebar “Fourier coefficients of a switch-matrix mixer,”). You can combine this filter with the ADC’s antialiasing filter.

A low-IF-receiver architecture has adjacent channels in the negative-frequency range of the desired signal (Figure 3). A real antialiasing filter can filter out only adjacent Channel 2. Adjacent Channel 1 is the image of the desired channel and passes through the antialiasing filter without attenuation. The antialiasing filter must be good enough to prevent aliasing from adjacent Channel 2. The ADCs require a dynamic range greater than 70 dB.

The addition of the switch-matrix mixer moves the desired signal into the baseband (Figure 4). The antialiasing filter must filter out not only the adjacent channels but also the mixing terms from the harmonics of the switching function. In this case, however, the antialiasing filter’s bandwidth is half that of the previous case. Maintaining the same filter order results in a sharper antialiasing filter. The filter suppresses both adjacent channels, dramatically reducing the ADC’s required dynamic range.

Other channels outside the adjacent channels may fall into the baseband due to mixing with the harmonics of the switch function. To address this problem, you must apply an image filter in front of the switch-matrix mixer. This filter is more relaxed than the antialiasing filter. Both adjacent channels are filtered, so the antialiasing filter allows the ADC to have a lower number of bits.

**Simulation results**

You can do a simulation using The MathWorks Matlab to illustrate the process of an ideal low-IF mixer (Figure 5). You can simulate a 100-kHz RF signal with a strong interferer at 70 kHz. The spectrum at this point is symmetric, corresponding to a real signal. A complex-valued mixer shifts down the signal to the low IF, making the spectrum asymmetric. An interferer signal appears at the image frequency with respect to zero. Derotating with the remaining IF yields a zero-IF baseband signal. You can filter away the interferer using a real-valued filter.

You can also simulate an ideal switch-matrix mixer (Figure 6). The first two plots are the same as those in Figure 5 because the switch-matrix mixer replaces only the low-IF derotation process. The third plot depicts that, even with perfect switches, some spectral interleaving occurs. You can separate these interlaced higher-order products using filtering, as the bottom plot shows. Introducing a gain error causes even more spectral interleaving (Figure 7). These additional subbands are filtered off and do not cause a problem. However, I/Q imbalance results in the usual image problem, quantitatively of the same order as with any low-IF mixer.
A prototype PCB (printed-circuit board) of the switch-matrix mixer includes the clock-phase generators (Figure 8). Lowpass filters surround the switch-matrix mixers. You mix a 2.40002-GHz RF signal, which is 20 kHz offset from 2.4 GHz, with a 20-kHz IF using a Maxim MAX2701 image-rejection mixer. You send the I and the Q part of the low-IF signal to the test board. It downconverts the signal to a baseband signal using a clock frequency of four times 14 kHz to get four phases, resulting in 56 kHz. After the first mixing process, the resulting frequency spectrum of this signal has three peaks (Figure 9). One peak is the image at −20 kHz, or 40 dB down. The second peak is the dc offset. The third peak is the signal of interest at 20 kHz.

After the second mixing process, the signal of interest now shifts to 6 kHz (Figure 10). The previous dc peak shifts to −14 kHz, and the switch-matrix mixer generates a new dc-offset peak; 40 dB also suppresses the image of the switch-matrix mixer at −6 kHz. Choose the cutoff frequencies of the lowpass filters before and after the switches as 30 and 15 kHz, respectively.

A switch-matrix mixer reduces the dynamic range needed in a subsequent ADC. Apart from the switches, only an additional low-order filter is necessary to prevent unwanted harmonics from falling into the baseband. You can integrate these functions into a single IC.
References

5. Pun, Kong-Pang; JE da Franca; C Azeredo-Leme; and R Reis, “Quadrature sampling schemes with improved image rejection,” IEEE Transactions on Circuits and Systems—II, Volume 50, No. 9, September 2003, pg 641.