Spread-spectrum clocking reduces EMI in embedded systems

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For years now, government institutions have been regulating the amount of EMI (electromagnetic interference) an electronic device or system can emit. Their efforts primarily target lowering dissipated power and eliminating any interference to the function of other surrounding devices as a result of EMI. Spread-spectrum clocking is a popular implementation for reducing EMI in synchronous systems.

Spread-spectrum-clocking benefits

EMI is the energy resulting from a periodic source in which most of the energy becomes a single fundamental frequency. The influence of these unwanted signals can manifest itself in the limited operation of other devices and systems. In some cases, the EMI-generated disturbance can make it impossible for these devices or systems to operate. Because an electromagnetic signal must have a source, synchronous systems are ideal candidates for generating excessive EMI. Within a system, the coupling paths in PCBs (printed-circuit boards) transmit the generated EMI that affects other system components. However, EMI can occur even in the absence of a conductive medium, such as an electric conductor or dielectric. In most cases, EMI results from a combination of conduction and radiation.

The primary PCIe (PCI Express) model implements a synchronous-clocking scheme. That is, the same 100-MHz clock source generates the reference clock for PCIe devices. Furthermore, in the case of a motherboard, the traces on the PCB can act as coupling paths to facilitate the transmission of EMI to the surrounding devices. The disturbance that occurs can affect not only the system but also other surrounding systems when EMI travels through the atmosphere in the form of radiation.

One method of minimizing the EMI that a device generates is to keep the disturbing signals below a certain level. You accomplish this goal by modulating the disturbing signals across a wider frequency range, thus spreading the energy across a range of frequencies rather than concentrating it at one frequency. In PCIe systems, the modulation of the reference clock is spread-spectrum clocking.

The most common modulation techniques are center-spread and down-spread. The center-spread approach applies the modulated signal in such a way that the nominal frequency sits in the center of the modulated frequency range. That is, half of the modulated signals deviate above the nominal frequency, and the other half deviate below it. A down-spread approach also results in a range of deviated frequencies. However, in the down-spread approach, the modulated signals deviate below
the nominal frequency.

Many PCIe systems implement EMI-minimizing spread-spectrum clocking by spreading the spectral energy of the clock signal over a wide frequency band. In spread-spectrum-clocking systems, PCIe components generally must use a reference clock from the same source. This approach allows a transmitter PLL (phase-locked-loop) and a receiver-clock-recovery function, or clock-data-recovery circuit, to track the modulation frequency and remain synchronous with each other. If only one side of the link uses a spread-spectrum-clocking reference clock, the transmitter and receiver circuits cannot properly track one another. For example, if a PCIe add-in card interfaces to a spread-spectrum-clocking system and also implements a cable connection to a downstream card that is using a constant-frequency-clock source, the downstream interface will be unable to connect.

The PCIe base specification provides guidelines for modulating the reference-clock input to PCIe devices. At a high level, the PCIe specification uses the down-spread approach when using a 30- to 33-kHz-wave signal as the modulating frequency to the 100-MHz clock, resulting in a frequency range of 99.5 to 100 MHz (Figure 1).

**Isolation in PCIe switches**

To solve a link-up problem due to mixing spread-spectrum- and constant-frequency-clocking implementations, designers must provide a means to pass the spread-spectrum clock to all of the devices. This task poses a challenge in modular systems at both the physical and the electrical levels. A better option would be to use the spread-spectrum-clocking isolation function available in select PCIe switches (Figure 2). These switches provide an isolation feature that helps eliminate the issue of trying to communicate between two systems when one or both of those systems use spread-spectrum clocking.

The switch has the necessary buffering and logic required to allow the upstream port to operate using both a spread-spectrum-clocking and a constant-frequency-clock source. You can use strapping options to enable this feature in the switch. When you enable the switch, its Port 0 operates in the spread-spectrum-clocking domain, and the other ports operate in the constant-frequency-clock domain. The ability of the switch to function in two clock domains provides system designers flexibility in expanding modular systems using cable, as well as simplifying the overall system-clocking scheme.

The separation of clock domains delivers numerous benefits, including the reduction of phase jitter.
and the ability to link systems with independent clocking sources. With this ability, the use of a nontransparent bridge becomes more flexible. Because of the clocking requirements of PCIe, few system architectures can take advantage of nontransparent bridges. Their primary use has been in embedded systems using the second root-complex subsystem in a fault-tolerant or fail-over application or in RAID (redundant-array-of-inexpensive-disk) controllers. In both cases, the secondary system still connects to the primary in clocking architecture; therefore, the approach has limited flexibility because all system components using PCIe must use the same clocking source.

With the ability to separate clock domains, independent systems can link because the secondary clock domain is independent of the primary domain. With this capability and the use of nontransparent bridges, two or more PCs can connect over PCIe, and most of the systems can operate in a reduced-emissions mode. Using low-cost PCIe hardware, a new high-speed, low-latency interface creates a powerful computing environment.

One application of this environment may be a switch module in a blade-server chassis (Figure 3). With the constant-frequency clock on the module side and each blade using off-the-shelf components, the blade system becomes a low-cost supercomputer without the latency and bandwidth limitations of Ethernet or the cost and complexity issues of InfiniBand. The use of the isolated-clock domains enables new application for systems using standardized components. The new PXI (PCI extensions for instrumentation) multicomputing specification employs this technology.

The other benefit of using independent clock domains is to reduce phase jitter. For PCIe systems, phase jitter is the accumulation of nonideal frequency components in the reference clock that spread to PCIe devices. General-purpose computing platforms typically employ cost-effective clocking architectures. For systems that provide expansion capabilities, such as cabled expansion chassis, the phase jitter is a key parameter for interoperability.

This fact is important because the energy in the nonideal frequencies of the clock adds up to the time-domain jitter profile. Certain frequencies contribute to the jitter in the link budget. As distance between the devices increases, the time-domain jitter changes behavior and usually increases. The common implementations for PCIe provide a 12-nsec delay for phase-jitter analysis. In cabled interfaces, this delay ranges from 10 to 70 nsec. In addition, buffering the reference clock adds jitter to the signal. This unpredictable behavior of the reference clock requires an approach that provides a degree of certainty for the link budget. Isolating the expansion reference clock from the system’s cost-effective clocking circuits greatly reduces interoperability issues. As the interest in general-purpose graphics processors enhances the computational capabilities of a single system, expansion systems’ additive jitter will become an issue that clock-domain isolation can address.