Genesys Logic Selects nSys for SuperSpeed USB Verification

EDN Staff - November 18, 2008

November 18, 2008 – nSys Design Systems Pvt. Ltd. (nSys), developers of the World’s largest portfolio of Verification IPs today announced that Genesys Logic, Inc. has licensed nVS (nSys Verification Suite) for SuperSpeed USB for the development of the SuperSpeed based designs. Genesys Logic engineers are using the nVS verification IP to simulate, and verify the USB 3.0 interface of the next generation Genesys Logic chips. The use of nVS will help the Genesys Logic team eliminate bugs at the pre-silicon stage at a much faster rate than they had anticipated, reducing time-to-market while having higher quality end products.

"The USB 3.0 nVS is providing us independent interpretation of the SuperSpeed USB specifications," said Tina Chen, VP Engineering at Genesys Logic. "The nVS is helping find bugs before the design is implemented in silicon. We have been using other Verification IPs from nSys for the last several years and the consistency of interface and operation across the nVS family helped us drastically reduce the learning curve and hence Accelerated our SuperSpeed USB based design."

Genesys Logic specializes in high speed I/O technology, specifically USB 2.0 and PCI Express chip technology development. In this area, Genesys Logic is one of Taiwan's most outstanding companies. "nSys is focused on providing industry leaders such as Genesys Logic with tools for verifying designs based upon SuperSpeed USB," said Atul Bhatia, CEO nSys Design Systems. "We are pleased to deliver USB 3.0 nVS to early adopters who are eager to verify their SuperSpeed USB designs."

About USB 3.0 nVS: The USB 3.0 nVS (nSys Verification Suite) is a complete verification solution consisting of Bus Function Model (BFM), Monitor, Checker and Test Suites for functional verification of all types of USB 3.0 based designs. The nVS allows design and verification engineers to quickly and extensively test the entire functionality of USB 3.0 compliant devices. Availability of Test Suites enables the designer to focus on features unique to the design. The nVS family of products are available in SystemVerilog (OVM/VMM) and Verilog. All the nVS family of products are integrated to work with popular languages/environments like 'e', SystemC, OpenVera and VHDL.

For more information and to register for Evaluation license of USB 3.0 nVS, visit: www.nsysinc.com/usb3

Availability: The USB 3.0 nVS is available now for all popular simulators and verification environments.

About nSys: nSys leverages the world’s largest portfolio of Verification IPs it has developed, to provide products & services to Accelerate Designs of its customers developing ASIC or FPGA. The nVS family has proven VIPs for standard interfaces such as PCI Express, Ethernet, SATA, SAS, AXI, USB, SDIO, DDR3, DDR2 etc. For more information, please visit www.nsysinc.com

About Genesys Logic: Established 1997 in Taipei County, Taiwan, Genesys Logic’s primary business is the design and research and development of electric circuits, semiconductors, digital communications products, computer peripherals, and other related products. Genesys Logic
specializes in high speed I/O technology, specifically USB 2.0 and PCI Express chip technology development. In this area, Genesys Logic is one of Taiwan's most outstanding companies.

In the USB market, Genesys Logic makes use of its own core technology design, aside from computer market applications; Genesys Logic has also applied the technology in consumer electronics and telecommunications products.
For more information, please visit Genesys Logic, Inc. at www.genesyslogic.com

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