Implementing an SLVS transceiver

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Over the past two decades, the explosive growth in demand for data bandwidth has led to a variety of data-transmission standards. Lower implementation costs and the ability to transfer more data bits with less power consumption are the primary goals of any data-transmission standard. Since National Semiconductor’s introduction of LVDS (low-voltage differential signaling) in 1994, it has become the most widely adopted data-transceiver standard in the industry for delivering gigabit performance levels at milliwatt power levels.

Although the company crafted the technology for easy implementation in the equipment of a previous decade, it has its limitations. Addressing the limitations of LVDS as a generic standard, several variations have evolved to meet application-specific requirements. In October 2001, the JEDEC (Joint Electron Device Engineering Council) Solid State Technology Association published the SLVS (scalable-low-voltage-signaling) standard for 400-mV operation. SLVS inherits from LVDS low noise susceptibility. It also boasts a scaled-down 400-mV signal swing—versus the 700-mV swing of LVDS—and includes a ground reference. This combination results in lower power consumption for transmission. The interface normally requires a 0.8V power rail, which is commonly available in submicron silicon devices. Designers can achieve a data rate as high as 3 Gbps or beyond over a range that is compatible with the size of a typical PCB (printed-circuit board). This combination of features makes SLVS appropriate for use in high-speed, low-power transmission for interdevice data links on a PCB.

This utility also makes SLVS important in the FPGA world. Designers often use FPGA devices, due to their feature-rich I/O ports, for datapath interfacing and protocol bridging. With the increasing popularity of SLVS in data-channel design, designers hope to achieve economic and robust FPGA design for SLVS-transceiver applications. Most FPGAs support the traditional LVDS interface. However, designers cannot program all modern FPGA-I/O structures to drive current at SLVS requirements for output, and not all provide a built-in differential termination to receive SLVS input with few external components. To determine the abilities of an FPGA-I/O design to support SLVS, you must look deeper into both the standard and the I/O structures that today’s programmable devices use.

LVDS/SVLS overview

The LVDS data-transmission standard is a mature technology and has become the most common transceiver interface in applications such as video, storage, and data
communications, which require transmission of large amounts of data. In a point-to-point LVDS link, a current source in the transmitter toggles polarity as the signal changes state, driving the wire loop (Figure 1). Most of the drive current flows through the receiver-side termination resistor, assuming high impedance at the op amp’s input for dc current. The voltage drop across the termination resistor is proportional to the drive current; when the transmitter toggles, the receiver’s op amp detects the change in polarity, recognizing the change in signal state at the transmitter’s input.

LVDS offers high noise tolerance because it uses a pair of differential traces to provide common-mode rejection. Both the speed of data transmission and the power dissipation closely relate to the voltage swing across the termination resistor, which is 350 mV, or 700 mV p-p nominal, over a 100Ω resistor for a typical LVDS loop.

LVDS channels have a low susceptibility to external noise because distant noise sources tend to add the same amount of voltage to both lines, so the difference between the voltages remains the same. The low common-mode voltage is the average of the voltages on the two traces—approximately 1.25V. The transmitter sets the common-mode voltage as an offset voltage from ground. The 350-mV differential voltage causes the LVDS to consume static power in the LVDS load resistor, depending on the 1.25V offset voltage and 350-mV differential-voltage swing.

The JEDEC JESD8-13 SLVS-400 standard defines a point-to-point signaling method. SLVS uses smaller voltage swings and a lower common-mode voltage than LVDS. The 200-mV, or 400-mV-p-p, SLVS swing contributes to a reduction in power and is common in RSDS (reduced-swing-differential-signaling) standards. The RSDS standard reduces the swing from 350 mV to 200 mV with the same 1.25V common-mode offset of the LVDS standard. SLVS goes further and also reduces the common-mode voltage. The SLVS nominal common-mode voltage of 200 mV provides a considerable decrease in quiescent power. The combination of a smaller signal swing and low common-mode voltage produces much lower power consumption.

To illustrate this point, consider that a 6-Gbps LVDS SERDES (serializer/deserializer) link consumes approximately 250 mW. A typical SLVS pair running at 800 Mbps consumes approximately 15 mW. Even eight 800-Mbps SLVS links running in parallel for a combined speed of 6.4 Gbps consume only about 120 mW—less than half the power consumption of the LVDS implementation.

**FPGA design for SLVS**

To build an SLVS-compatible interface, a designer must consider whether the target FPGA device provides sufficient hardware resources and flexibility at its I/O ports for both receiver and transmitter implementation. Embedded differential termination is preferable in an SLVS receiver to minimize the number of onboard components that directly connect to its transmitter peer. More important, many FPGA receivers target use in LVDS, so designers should ensure that the FPGA receiver’s differential and common-mode range covers the entire SLVS output specification. The FPGA’s differential output port also must be able to source the drive current for the proper SLVS level with an external coupling-resistor network.

Like LVDS, SLVS requires a load termination at the receiver but does not specify whether the termination is inside or outside the receiver. Most FPGA devices typically use both built-in and board resources to build an SLVS interface to industry-standard devices. To achieve cleaner board interconnections and robust system performance, an FPGA device that contains built-in differential termination in the receiver implementation has an advantage (Figure 2).
The programmability of the output current source is critical for an SLVS transmitter. You must program the differential driver current to a value that emulates SLVS requirements. The design typically uses an onboard resistor network to adjust the swing and common-mode voltages that the SLVS receiver requires. To compensate for the power consumption of the onboard resistor network, the current-source driver buffer typically must inject more than the LVDS-nominal 3.5 mA of current into the off-chip differential traces. A current-driver buffer meeting this requirement is not commonly available with a traditional LVDS-compatible FPGA-I/O port.

One SLVS-interface implementation uses an FPGA in which the features of the LVDS inputs conform to the signaling requirements to directly connect to SLVS transmitters (Figure 3). The internal differential terminations are available for inputs on all sides of the device. Common-mode- and differential-voltage ranges sufficiently cover the SLVS output spec, enabling the inputs to receive data streams as fast as 2 Gbps without any additional board components. The FPGA also provides programmability of differential-current output at 2, 3.5, 4, and 6 mA. This example uses a 6-mA driver current with the off-chip termination circuitry to emulate the SLVS requirements. Table 1 details SLVS-specification conformance for this example.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Device LVDS Input (mV)</th>
<th>SLVS output (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum common-mode voltage</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>Maximum common-mode voltage</td>
<td>2350</td>
<td>250</td>
</tr>
<tr>
<td>Minimum differential voltage</td>
<td>100</td>
<td>140</td>
</tr>
<tr>
<td>Maximum differential voltage</td>
<td>2400</td>
<td>270</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Output with resistor network (mV)</th>
<th>SLVS input (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum common-mode voltage</td>
<td>150</td>
<td>70</td>
</tr>
<tr>
<td>Maximum common-mode voltage</td>
<td>280</td>
<td>330</td>
</tr>
<tr>
<td>Minimum differential voltage</td>
<td>180</td>
<td>140</td>
</tr>
<tr>
<td>Maximum differential voltage</td>
<td>280</td>
<td>450</td>
</tr>
</tbody>
</table>
SLVS applications

The SLVS interface finds application in, for example, data communications and video/image displays requiring high-speed and low-power data channels. An FPGA device with SLVS-compatible transceivers plays an important role in bridging the SLVS I/O on a standard IC product to other data protocols. The recent design-in of a Lattice SC/M FPGA with a Broadcom VDSL2 (very-high-bit-rate-digital-subscriber-line) reference line card demonstrates how the FPGA provides SLVS interfacing and XAUI (10-Gbps-attachment-unit-interface) PHY (physical)-layer bridging functions.

On the VDSL2 reference design, the FPGA implements six SLVS links (Figure 4). The FPGA device functions as a bridge between the SLVS data stream and the XAUI packets. The VDSL2 device transmits three links and receives three links. Each link contains an 18-bit bus, connecting to the standard SLVS ports from Broadcom’s DSL (digital-subscriber-line)-termination ICs to the FPGA. The FPGA can steer and multiplex the SLVS buses from any of the three receiver links to any of the three transmitter links, so the Broadcom devices all interconnect. At the other side of the FPGA, eight 3.125-Gbps SERDES channels can form two interfaces for Ethernet-switch connections. This configuration constructs a typical 48-line VDSL2 terminal in a 10-Gbps backhaul connection.

![Figure 4 An FPGA bridges between an SOC with SLVS I/O and a set of XAUI ports.](Click to enlarge)

The differential I/Os on the FPGA support a data-transmission speed of 884 Mbps. Along with built-in LVDS transceivers and XAUI-sublayer logic, the FPGA internally implements two buffering and packet-conversion function blocks and two Ethernet MAC (media-access-control) blocks. All four of these blocks consume less than 15,000 look-up tables. This relatively high ratio of SERDES-to-look-up-table resource requirements is characteristic of many implementations of high-speed SLVS bridging in DSLAM (digital-subscriber-line-access-multiplexer) applications. Along with adequate I/O flexibility to implement robust SLVS ports, it is useful for the FPGA family to have members that emphasize high-speed-I/O-pin count rather than logic-cell count.

A number of features, including low differential-mode signal swing and low common-mode voltage, provide lower power dissipation for SLVS ports than that of LVDS ports. This advantage is leading to wide use of SLVS within the communications/networking community, especially on the latest generation of SOCs (systems on chips). FPGAs provide a flexible and economical implementation for a data-transmission interface and for protocol bridging, so it is important for designers to understand how to implement an SLVS interface in an FPGA. Design engineers should carefully consider an FPGA’s I/O features and select the right device from commonly available LVDS-
compatible systems to implement the lower-power SLVS interface. Features such as wide input common-mode range, built-in differential-termination load, programmable SLVS drive-current output, and high SERDES-to-logic ratios can have a substantial effect on board-level implementation of SLVS links.

**References**