Discontinuous conduction brings issues to current-mode converters

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Control loops for power converters are complex and rely on the converter’s operation within a window of defined conditions. However, when converters operate outside these defined conditions, they can exhibit unexpected behavior. This article explores one of the most common problems design engineers face: moving a forward buck converter from the normal defined operational window of continuous conduction into a lightload condition of discontinuous conduction.

You develop the control loop around a mathematical model of a buck converter (Figure 1). Established models exist for both current- and voltage-mode switching buck converters. For this model, you assume sufficient load current so that the current through the inductor is continuous. If you ignore losses and semiconductor voltage drops, the output voltage is equal to the input voltage factored by the turns ratio times the duty cycle. The primary-to-secondary turns ratio is 1-to-N. Ignoring diode and FET voltage drops, the voltage at the junction of the diodes when the switch is on is the input voltage times N.

You now increase the load impedance to the point that the current through the output inductor is no longer continuous. Your basic assumption is then no longer valid. In this case, the control theory that relates to the continuous model is inaccurate, and the converter begins discontinuous operation, during which the current moving through the inductor to the output is discontinuous. The output inductor sometimes does not connect to the transformer winding or to ground through a diode. When the primary-side switch is on, the current through the output inductor increases linearly. The slope is a function of the voltage across the inductor. When the switch turns off, the current through the inductor tries to continue, causing the voltage to drop and pulling current through the diode that connects to ground. With the reversal of voltage across the inductor, the current through the inductor starts to decrease. In discontinuous operation, the current falls to 0A.

The average current in the output inductor must equal the load current. You can write a series of equations to define the circuit in continuous mode. First, ignore diode and FETswitch voltage drops. When the FET is on, the voltage at the input to the output inductor, $L_{\text{OUT}}$, is $V_{\text{IN}} \times N$. You can then define the output as a function of input voltage; duty cycle, D; and transformer turns ratio, N:
You can now calculate the peak current through the inductor:

\[ I_{pk} = I_{dc} + 0.5 \times \frac{L_{out}}{(V_{in} \times N) - V_{out} \times D} \times \frac{1}{F_{sw}} \]

where \( F_{sw} \) is the switching frequency. The integral of the current through the inductor must equal the total load current for the cycle, thus preventing a net change in the output voltage.

In a continuous-current-mode forward converter, a slight change in the inductor current accumulates over the total cycle time, changing the charge that the converter transfers to the output. In discontinuous operation, the change in current has less effect because it conducts for only a small percentage of the time, resulting in a change to the gain of the circuit and a change in the circuit dynamics. You use a different mathematical model to represent discontinuous-converter operation.

You can plot the output impedance of the converter over frequency for two load values (Figure 2). Given the assumed circuit values, the converter remains in continuous-conduction mode. Once you select a turns ratio for the transformer and a control IC, you can design the control loop, which has a gain from your theoretical control to the output voltage. You can chart that gain over frequency for both load conditions (Figure 3).

You should design the output-to-control feedback loop so that the gain will be one at your desired crossover frequency. The slope of the gain at this point of the gain curve is 20-dB—a factor-of-10—roll-off per decade. If you chose a crossover at 5 kHz, the control-to-output gain is 0.5, meaning that your feedback loop should have a gain of two at 5 kHz.
First, establish the feedback components from the control IC’s COMP pin back to the sensor/amplifier. You must take into account the range of voltage that the COMP pin requires. This portion requires a constant gain of four. The error-amplifier sensor circuit must have a gain of 0.5 at 5 kHz, and the gain should be nearly flat at 1 and 25 kHz. You tailor the gain shape around the error amplifier (Figure 4). The optocoupler and other circuitry must multiply the gain by a factor of four to compensate for the 0.5 gain of the error amplifier at 5 kHz. You accomplish this task by setting a gain of two through the optocoupler and two in the internal error amplifier in the PWM (pulse-width-modulation)-controller IC.

The optocoupler model employs real devices that have current-transfer-ratio variations of 50 to 200%. You can plot the loop gain over frequency for the optocoupler’s extreme and nominal current-transfer ratios (Figure 5). You plot the phase shift of the loop to verify the stability of the converter (Figure 6). The converter has more stability if it has more than 40° of phase margin when the loop gain crosses one.

**Figures 1 through 6** represent stable operation using a model with continuous current through the output inductor. When the load decreases, the inductor current becomes discontinuous. The high-frequency impedance of the converter remains the same, but the low-frequency impedance increases (Figure 7). If the dc-load resistance increases to 50Ω, the converter supplies a current of 0.2A.

For each cycle of a converter operating at 100 kHz, the load requires a 2-μC charge, Q. This charge arrives at the output in the form of a triangle of current with a definable upward slope based on the input voltage’s turns ratio, the output voltage, and a definable downward slope based on the output voltage (Figure 8). Because the current peak is common and a function of the on time, the upward and downward slopes are ratios of each other.
Again, ignore diode and FET voltage drops. You can relate the off time to the on time and the slopes with the following equation:

\[ T_{\text{OFF}} = \frac{T_{\text{ON}} \times \text{UPSLOPE}}{\text{DOWNSLOPE}} \]

where \( T_{\text{OFF}} \) is the off time, \( T_{\text{ON}} \) is the on time, UPSLOPE is the upward slope, and DOWNSLOPE is the downward slope. You can use this equation to determine \( Q \), the charge per cycle:

\[ Q = \frac{I_{\text{OUT}}}{F_{\text{SW}}} - 0.5 \times \text{UPSLOPE} \times T_{\text{ON}} \times (T_{\text{ON}} + T_{\text{OFF}}) - \frac{0.2A}{F_{\text{SW}}} = 2 \mu \text{C}. \]

You define the upward slope by relating the input voltage, the turns ratio, and the output voltage:

\[ \text{UPSLOPE} = \frac{V_{\text{IN}} \times N \times V_{\text{OUT}}}{I_{\text{OUT}}} = \frac{75V}{N_{\text{PRI}}} - \frac{10V}{I_{\text{OUT}}} = 0.429A/\mu\text{SEC}, \]

where \( N_{\text{PRI}} \) is the reciprocal of the transformer’s primary turns. The downward slope of the inductor current depends on the output voltage and the inductor value:

\[ \text{DOWNSLOPE} = \frac{V_{\text{OUT}}}{I_{\text{OUT}}} = \frac{10V}{I_{\text{OUT}}} = 0.13A/\mu\text{SEC}. \]

You can combine the above equations and rearrange them to solve for the on time:

\[ T_{\text{ON}} = \frac{2 \times Q \times \text{DOWNSLOPE}}{\text{UPSLOPE} \times (\text{UPSLOPE} \times \text{DOWNSLOPE})} = 1.476 \mu\text{SEC}. \]

From these equations, you can calculate the peak secondarieside current:

\[ I_{\text{PK}} = \frac{T_{\text{ON}} \times \text{UPSLOPE}}{0.632A}, \]

where \( I_{\text{PK}} \) is the peak current. Because you have chosen a turns ratio, you can infer the primary-side peak current. This secondary peak current translates to the primary side through the power transformer and the current-sense transformer to the current-sense resistor. (Click here for a)
A detailed schematic of this design.) With a UCC2813-2 controller, it represents a voltage of 1.435V on the COMP output. This voltage includes offsets and internal IC gain. You next remove any offsets to identify the contribution of the current within this voltage. The portion of the COMP voltage due to the peak current is 0.085V.

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The dc gain of the control to the output is the output voltage divided by the primary current-sense voltage. In this case, the output voltage is 10V; divided by the peak current, it yields 0.085V, or 117.255V. You can now determine the complete open-loop gain and phase (Figure 9). This figure includes the gain of the error amplifier as well as that of the other circuit parameters. The change in output load changes the loop gain as well as the phase response.

In this converter design, the loop 0-dB gain-crossover frequency decreases from 5 kHz with approximately 120° of phase margin to a 0-dB gain-crossover frequency at 1 kHz and 60° of phase margin. With this design, the converter is stable under both conditions, but the change is significant.

Now consider a case in which the current-transfer ratio of the optocoupler is low (Figure 10). The 0-dB loop crossover is 600 Hz, and the phase margin is 45°. This marginal amount means that the control loop is still stable. The variable parameter of current-transfer ratio might mean that a design that is stable under normal continuous operation will have problems in discontinuous mode. As the current-transfer ratio of the optocoupler degrades over time, your designs could have problems in discontinuous mode. You should test the stability of the unit under minimum-load conditions in case any unexpected issues arise with the discontinuous current through the output inductor. Build your designs with margins to handle these conditions.