Design a 100A active load to test power supplies

Jim Williams - September 22, 2011

You use an active-load test circuit to ensure that a power supply for a microprocessor or for other digital loads supplies 100A transient currents. This active load can provide a dc load for a power supply, and it can rapidly switch between dc levels. These transient loads simulate the fast logic switching in the microprocessor.

Ideally, your regulator output is invariant during a load transient. In practice, however, you will encounter some variations, which become problematic if allowable operating-voltage tolerances are exceeded. You can base your active-load circuit on previous designs of wideband loads that operate at lower currents (Reference 1). This approach allows you to design a closed-loop, 500-kHz-bandwidth, 100A active load having linear response.

Conventional active-load circuits have shortcomings (Figure 1). The regulator under test drives dc and switched resistive loads. Monitor the switched current and the output voltage so that you can compare the stable output voltage versus the load current under both static and dynamic conditions. The switched current is either on or off. You cannot control it in the linear region as it changes.

You can further develop the concept by including an electronic-load switch control (Figure 2). The input pulse switches the FET through a drive stage, generating a transient load current from the regulator and its output capacitors. The size, composition, and location of these capacitors have a profound effect on transient response. Although the electronic control facilitates high-speed switching, the architecture cannot emulate loads that are between the minimum and the maximum currents. Additionally, you are not controlling the FET’s switching speed because doing so
introduces wideband harmonics into the measurement that may corrupt the oscilloscope display.

![Figure 2](image2.png) A conceptual FET-based load tester permits step loading. Switched current is either on or off; there is no controllable linear region.

![Figure 3](image3.png) A feedback-controlled load-step tester allows continuous FET-conductivity control.

**Transient generator**

Placing Q₁ within a feedback loop allows true, linear control of the load tester (Figure 3). You can now linearly control Q₁’s gate voltage, allowing you to set an instantaneous transient current at any point and to simulate nearly any load profile. Feedback from Q₁’s source to control amplifier A₁ closes a control loop around Q₁, stabilizing its operating point. The instantaneous input-control voltage and the value of the current-sense resistor set Q₁’s current over a wide bandwidth. You use the dc-load-set potentiometer to bias A₁ to the conduction threshold of Q₁. Small variations in A₁’s output result in large current changes in Q₁, meaning that A₁ need not supply large output excursions. The fundamental speed limitation is the small-signal bandwidth of the amplifier. As long as the input signal stays within this bandwidth, Q₁’s current waveform is identical in shape to A₁’s input control voltage, allowing linear control of the load current. This versatile capability permits you to simulate a wide variety of loads.

You can improve this circuit by adding some components (Figure 4). A gate-drive stage isolates the control amplifier from Q₁’s gate capacitance to maintain the amplifier’s phase margin and provide low delay and linear current gain. A gain-of-10 differential amplifier provides high-resolution sensing across the 1-mΩ current-shunt resistor. You can design a power-dissipation limiter that acts on the averaged input value and Q₁’s temperature. It shuts down the FET’s gate drive to preclude excessive
heating and subsequent destruction. Capacitors can be added to the main amplifier to tailor the bandwidth and optimize the loop response.

You can develop a detailed schematic based on these concepts (Figure 5). The main amplifier, $A_1$, responds to dc and pulse inputs. You also send it a feedback signal from $A_3$ that represents load current. $A_1$ sets $Q_1$’s conductivity through the $Q_4/Q_5$ gate-drive stage, which is actively biased using $A_2$. The voltage drop across the gate drive’s input diodes would be high enough to fully turn on $Q_4$ and $Q_5$. To prevent this overdrive, reduce the voltage across the lower diode with $Q_3$. Amplifier $A_2$ determines the gate-drive-stage bias by comparing $Q_4$’s averaged collector current with a reference and controlling $Q_3$’s conduction, thus closing a loop. That loop keeps the voltage drop across the bases of $Q_4$ and $Q_5$ to a value well under 1.2V, and servos that value until $Q_4$ and $Q_5$ have a 10-mA average collector-bias current.
The duty cycle of the load overheats if it is on for too long. You can fashion a protection circuit with techniques that high-power-pulse-generator designers use (references 2, 3, and 4). Feed comparator IC1 the average input-voltage value. It compares that voltage to a reference voltage set with the dissipation-limit-adjust potentiometer. If the input duty cycle exceeds this limit, comparator IC1 turns off the FET gate drive through Q2. Thermal switch S1 provides further protection. If Q1’s heat sink gets too hot, S1 opens and disconnects the gate-drive signal. By diverting Q4’s bias voltage, transistor Q6 and the zener diode prevent Q1 from turning on if the −15V supply is not present. A 1-kΩ resistor on A1’s positive input prevents amplifier damage should you lose the 15V power supply.
Trimming optimizes the dynamic response, determines the loop’s dc baseline idle current, sets the dissipation limit, and controls the gate drive’s stage bias. The dc trims are self-explanatory. The loop-compensation and FET-response ac trims at A1 are subtler. Adjust them for the best compromise between loop stability, edge rate, and pulse purity. You can use A1’s loop-compensation trimming capacitor to set the roll-off for maximum bandwidth and accommodate the phase shift that Q1’s gate capacitance and A3 introduce. The FET-response adjustment partially compensates Q1’s inherent nonlinear-gain characteristic, improving the front and rear pulses’ corner fidelity (see sidebar “Trimming procedure”).

Circuit testing

You initially test the circuit using a fixture equipped with massive, low-loss, wideband bypassing (Figure 6). It is important to do an exceptionally low-inductance layout in the high-current path. Every attempt must be made to minimize inductance in the 100A path. You should get good results after you properly trim the circuit if you minimize inductance in the high current path (Figure 7). The 100A-amplitude, high-speed waveform is pure, with barely discernible top-front and bottom-rear corner infidelities (see sidebars “Verifying current measurement” and “Instrumentation considerations”).
To study the effects of ac trim on the waveform, you must perform deliberate misadjustments. An overdamped response is typical of excess $A_1$ feedback capacitance (Figure 8). The current pulse is well-controlled, but the edge rate is slow. Inadequate feedback capacitance from $A_1$ decreases the transition time but promotes instability (Figure 9). Further reducing the trim capacitance causes loop oscillation because the loop’s phase shift causes a significant phase lag in the feedback. Scope photos of uncontrolled 100A loop oscillation are unavailable. The event is too thrilling to document. Overdoing the FET’s response compensation causes peaking in the corners of the waveform (Figure 10). Restoring the ac trims to nominal values causes a 650-nsec rise time, equivalent to a 540-kHz bandwidth, on the leading edge (Figure 11). Examining the trailing edge under the same conditions reveals a somewhat-faster 500-nsec fall time (Figure 12).
If parasitic inductance is present in the high-current path, your design cannot remotely approach the previous responses. You can deliberately place a tiny, 20-nH parasitic inductance in Q\textsubscript{1}’s drain path (Figure 13), which will cause an enormous waveshape degradation deriving from the inductance and the loop’s subsequent response (Figure 14a). A monstrous error dominates the leading edge before recovery occurs at the middle of the pulse’s top. Additional aberration is evident in the falling edge’s turn-off. The figure’s horizontal scale is five times slower than the optimized response (Figure 14b). The lesson is clear: High-speed 100A excursions do not tolerate inductance.

**Regulator testing**

After you address the compensation and layout issues, you can test your power-supply regulator (Figure 15). The six-phase, 120A LinearTechnology Corp LTC1675A buck regulator acts as a demonstration board. The test circuit generates the 100A load pulse (Trace A of Figure 16). The regulator maintains a well-controlled response on both edges (Trace B of Figure 16). The active...
load’s true linear response and high bandwidth permit wide-ranging load-waveform characteristics. Although the step-load pulse in Figure 16 is the commonly desired test, you can generate any load profile. A burst of 100A, 100-kHz sine waves is an example (Figure 17). The response is crisp, with no untoward dynamics despite the high speed and current. You could form a load even from an 80-μsec burst of 100A p-p noise (Figure 18). The load circuit has high accuracy, compliance, and regulation specifications (Figure 19 and Table 1).

![Graph showing load current vs. minimum Q, drain voltage]

**Table 1: Active-load Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Specification</th>
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<tr>
<td>Current accuracy (referred to input)</td>
<td>1% full-scale</td>
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<tr>
<td>Temperature drift</td>
<td>100 ppm/°C of reading +20 mA/°C</td>
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<tr>
<td>Current regulation versus supply</td>
<td>Greater than 60-dB power-supply-rejection ratio</td>
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<tr>
<td>Bandwidth</td>
<td>540 kHz at 100A with a rise time of 650 nsec, 435 kHz at 10A with a rise time of 800 nsec</td>
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<tr>
<td>Compliance voltages for full output current</td>
<td>0.95V minimum (see Figure 19); 70°C Q, thermal-dissipation limiter sets maximum</td>
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**Figure 19** Active-load characteristics feature small current-accuracy and regulation errors. The bandwidth mildly retards at low currents. The compliance voltage is less than 1V at 100A with 4% leading-edge overshoot and 1.1V with no overshoot.

**References**

**Author’s biography**
Jim Williams was a staff scientist at Linear Technology Corp, where he specialized in analog-circuit and instrumentation design. He served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). He enjoyed sports cars, art, collecting antique scientific instruments, sculpture, and restoring old Tektronix oscilloscopes. A long-time EDN contributor, Williams died in June 2011 after a stroke.

**Trimming procedure**
Trimming Figure 5’s circuit is a seven-step procedure that must be performed in order. Out-of-sequence adjustments are permissible if you have adjusted the dissipation-limiter circuitry.

1. Set all adjustments to midrange except A₁’s feedback capacitor, which should be at full capacity.
2. Apply no input. Bias Q₁’s drain from a 1V-dc supply. Turn on the power and trim the baseline current for 0.5A through Q₁. Monitor this current with an ammeter in Q₁’s drain line.
3. Turn off the power. Lift Q₂’s source lead and let it float, which disables the dissipation-limit circuitry, leaving Q₁ vulnerable to damage from inappropriate inputs. Follow the remainder of this step in strict accordance with the instructions. Turn on the power, bias Q₁’s drain from a 1V supply, apply a −0.1V-dc input, and monitor Q₁’s drain current with an ammeter. Trim the gain adjustment for a 10.5A meter reading. The trimming gain at only 10% of scale mandates the tight trim targets. This limitation is undesirable but less painful than trimming at 100% of scale, which would force astronomical—and brief—dissipation in Q₁ and the 1-mΩ shunt resistor. Make this adjustment fairly quickly because Q₁ dissipates 10W. Turn off the power and reconnect Q₂’s source lead. It is worth mentioning that the primary uncertainty necessitating gain trimming is the sense line’s mechanical placement at the 1-mΩ shunt resistor.
4. Turn on the power with no input and with Q₁’s drain unbiased. Trim the IQ adjustment for 10 mV at A₂’s positive input measured with respect to the −15V rail. Turn off the power.
5. Bias and bypass Q₁’s drain in accordance with Figure 6. Set the drain’s dc-power supply for 1.5V output and turn on the power. Apply a 1-kHz, −1V-amplitude, 5-μsec-wide pulse. Slowly increase the pulse width until IC₁ trips, shutting down circuit output and illuminating the power-limit LED. Tripping should occur at approximately a 12- to 15-μsec pulse width. If it does not, adjust the dissipation-limit potentiometer to bring the trip point within these limits. This step sets the allowable full-amplitude 100A duty cycle at approximately 1.5%.
6. Under the same operating conditions as those in Step 5, set the input pulse width at 10 μsec and adjust A₃’s capacitive trim for the fastest positive-going edge obtainable at A₃’s output without introducing pulse distortion. Pulse clarity should approach that in Figure 7 with somewhat degraded top-front and bottom-rear corner rounding.
7. Adjust the FET-response compensation to correct the corner rounding in Step 6. Some interaction may occur with Step 6’s adjustment. Repeat steps 6 and 7 until A₃’s output waveform looks like that in Figure 7.

Verifying current measurement

Theoretically, Q₁’s source and drain current are equal. Realistically, they can differ due to the effects of residual inductances and the 28,000-pF gate capacitance. A₃’s indicated instantaneous current could be erroneous if these or other terms come into play. You can verify that the source and the drain currents are equivalent (Figure A). Add a top-side, 1-mΩ shunt and a gain-of-10 differential amplifier to duplicate the circuit’s bottom-side current-sensing section. The results should eliminate concern over Q₁’s dynamic-current differences (Figure B). The two 100A pulse outputs are identical in amplitude and shape, promoting confidence in the circuit’s operation.
Instrumentation considerations

The pulse-edge rates in the main article are not particularly fast, but high-fidelity response requires some diligence. In particular, the input pulse must be cleanly defined and devoid of parasitics, which would distort the circuit’s output-pulse shape. A_1’s 2.1-MHz input RC (resistance/capacitance) network filters the pulse generator’s preshoot, rise-time, and pulse-transition aberrations, which are well out of band. These terms are not of concern. Almost all general-purpose pulse generators should perform well.

A potential offender is excessive tailing after transitions. Meaningful dynamic testing requires a rectangular pulse shape, flat on the top and the bottom within 1 to 2%. The circuit’s input band-shaping filter removes the aforementioned high speed-transition-related errors but does not eliminate lengthy tailing in the pulse flats. You should check the pulse generator for this issue with a well-compensated probe at the circuit input. The oscilloscope should register the desired flat-top- and flat-bottom-waveform characteristics. In making this measurement, if high speed-transition-related events are bothersome, you can move the probe to the band-limiting 300-pF capacitor. This practice is defensible because the waveform at this point determines A_1’s input-signal bandwidth.

Some pulse-generator output stages produce a low-level dc offset when their output is nominally at its 0V state. The active-load circuit processes such dc potentials as legitimate signals, resulting in a
dc-load baseline-current shift. The active load's input scale factor of 1V=100A means that a 10-mV zerostate error produces 1A of dc baseline-current shift. A simple way to check a pulse generator for this error is to place it in external-trigger mode and read its output with a DVM (digital voltmeter). If offset is present, you can account for it by nullifying it with the circuit's baseline-current trim. You could also use a different pulse generator.

Keep in mind parasitic effects due to probe grounding and instrument interconnection. At pulsed 100A levels, you can easily induce parasitic current into “grounds” and interconnections, distorting displayed waveforms. Use coaxially grounded probes, particularly at A3’s output-current monitor and preferably anywhere else.

It is also convenient and common practice to externally trigger the oscilloscope from the pulse generator's trigger output. There is nothing wrong with this practice; in fact, it is a recommended approach for ensuring a stable trigger as you move probes between points. This practice does, however, potentially introduce ground loops due to multiple paths between the pulse generator, the circuit, and the oscilloscope. This condition can falsely cause apparent distortion in displayed waveforms. You can avoid this effect by using a trigger isolator at the oscilloscope’s external-trigger input. This simple coaxial component typically comprises isolated ground and signal paths, which often couple to a pulse transformer to provide a galvanically isolated trigger event. Commercial examples include the Deerfield Laboratory 185 and the Hewlett-Packard 11356A. Alternatively, you can construct a trigger isolator in a small BNC-equipped enclosure (Figure A).

Figure A You can make a trigger isolator that floats input BNC’s ground using an insulated-shell BNC connector. A capacitively coupled pulse transformer avoids loading input, maintains isolation, and delivers the trigger to the output. A secondary resistor on T1 terminates ringing.