Basics of LRDIMM

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At the heart of the LRDIMM (load-reduced dual inline memory module) technology is the memory buffer. Figure 1 shows a high-level conceptual drawing of an LRDIMM, featuring one memory buffer on the front side of the memory module and multiple ranks of DRAM mounted on both front and back sides of the memory module.

![Memory Buffer](image)

**Figure 1: LRDIMM conceptual drawing featuring one memory buffer on the front side of the memory module and multiple ranks of DRAM mounted on both front and back sides of the memory module.**

The memory buffer re-drives all of the data, command, address and clock signals from the host memory controller and provides them to the multiple ranks of DRAM. The memory buffer isolates the DRAM from the host, reducing the electrical load on all interfaces. Reducing the electrical loading in this manner allows a system to operate at a higher speed for a given memory capacity, or to support a higher memory capacity at a given speed.

On existing RDIMM technology, the data bus connects directly to the multiple ranks of DRAM, increasing electrical load and limiting system speed as the desired server capacity increases. Figure 2 shows the system-level block diagram for RDIMM and LRDIMM.
To maximize module and system-level memory capacity and overcome limitations on the number of chip selects per channel, the LRDIMM supports Rank Multiplication, where multiple physical DRAM ranks appear to the host controller as a single logical rank of a larger size. This is done by utilizing additional row address bits during the Activate command as sub-rank select bits.

Read and Write commands do not require the additional sub-rank select bits, since the information is stored in the memory buffer after the Activate command. Rank Multiplication may be disabled, or set for 2:1 or 4:1 multiplication, up to a maximum of 8 physical ranks per LRDIMM.

**LRDIMM Features**

In addition to maximizing system memory capacity and speed, the LRDIMM architecture enables a number of useful features for the end-user. The LRDIMM’s memory buffer, the iMB, supports several useful features including DRAM and LRDIMM test features such as transparent mode and MemBIST (Memory Built-In Self-Test) functionality, VREF (voltage reference) margining for both the data (DQ) and command/address (CA) buses, parity checking for commands, in-band control word features similar to those of the 32882 register for RDIMMs, an optional out-of-band SMBus (Serial Management Bus) interface for LRDIMM configuration and status registers, and an integrated temperature sensor.

**Transparent mode:** For module testing purposes, the memory buffer can be placed in transparent mode, where it acts as a simple signal re-drive buffer and passes commands and data directly through to the DRAM devices.

**MemBIST:** For DRAM initialization and component testing purposes, the LRDIMM’s memory buffer supports a MemBIST (Memory Built-In-Self Test) function, enabling exhaustive at-speed testing of the DRAM devices. Testing can be performed at full operational speed, using either in-band (Command/Address bus) or out-of-band (SMBus) access.

**VREF margining:** LRDIMMs can use externally supplied voltage references for data (VREFDQ) and command/address signals (VREFCA), or supply the voltage references internally from the memory buffer. In the case when VREF is provided by the Memory Buffer, the voltage level can be controlled by the host though the Memory Buffer’s configuration registers. The programmable voltage references enable an LRDIMM memory system to utilize independent VREF voltage references for the host-to-DRAM interfaces and host-controller-to-memory-buffer interfaces and thus enable VREF margining to be independently performed for the host-to-DRAM interfaces and the host-controller-
o-memory-buffer interfaces. The independent VREF margining capability allows module and system suppliers to separately characterize and therefore guarantee the robustness of the signaling interfaces of the LRDIMM memory system.

**Parity checking:** To detect corrupted commands on the Command/Address bus, the memory buffer checks parity on the incoming commands and asserts an ERROUT_n signal if a parity error is detected.

**SMBus interface:** The memory buffer supports an out-of-band serial management bus to read and write configuration and status registers.

**Temperature sensor:** The memory buffer contains an integrated temperature sensor that is updated eight times per second and is accessible at any time through the SMBus. The memory buffer's EVENT_n pin can be configured as an interrupt back to the host to indicate high temperature events.

**How Does LRDIMM scale to higher speed?**
The benefits of the register component for RDIMMs are well known, and registered DIMMs provide system memory capacity advantages over unbuffered DIMMs. However, since the RDIMM's register component only buffers the command and address busses, the unbuffered data bus remains as a weakness for an RDIMM-based memory system. For example, a quad-rank DDR3 RDIMM presents four electrical loads on the data bus per RDIMM. Consequently, quad-rank DDR3 RDIMMs can only operate at a maximum data rate of 1066 MT/s in a one DIMM per channel (one DPC) configuration, and 800 MT/s in a two DIMM per channel (two DPC) configuration. LRDIMMs, which buffer the data bus along with the command and address busses, can operate at higher data rates and in higher memory density configurations.

Figure 3 shows the simulated eye diagram of the data bus with two quad-rank RDIMMs in a two DIMM per channel configuration. It demonstrates that with the presence of 8 electrical loads on the data bus, the signal integrity of the memory channel is severely degraded and limits the signaling rate of the memory system. Specifically, it shows that with eight electrical loads at 1333 MT/s, the maximum data eye width on the data bus is reduced to 212 ps at an idealized VREF point, and less than 115 mV at the maximum voltage opening.
Figure 3: A simulated eye diagram of the data bus with two quad-rank RDIMMs at 1333 MT/s shows that with the presence of eight electrical loads on the data bus the signal integrity of the memory channel is severely degraded.

The effect of this reduced data eye means that the two quad-rank RDIMMs in the two DIMM per channel configuration are not suitable for operation at 1333 MT/s. Figure 3 thus illustrates the difficult trade-off that memory system architects must face between higher capacity and higher data rate memory system operation in RDIMM memory systems.

Figure 4 shows the simulated eye diagram of the data bus with two quad-rank LRDIMMs in the two DIMM per channel configuration. With the electrical loads of the eight physical ranks of DRAM devices replaced with two electrical loads of the memory buffer on the data bus, the signal integrity of the data bus is greatly improved. Specifically, Figure 4 shows that under the same simulation conditions as that used for the two quad-rank RDIMMs in Figure 3, the maximum data eye width on the data bus is improved from 212 ps to 520 ps, and the maximum data eye height is improved to 327 mV from 115 mV at the maximum voltage opening.

Figure 4: A simulated eye diagram of the data bus with two quad-rank LRDIMMs at 1333 MT/s demonstrates the enabling of higher data rate operation for high-capacity memory modules.

The effect of this improved signal integrity means that the LRDIMM is able to operate at 1333 MT/s and above, even when multiple LRDIMMs are populated in the same channel. Figure 4 thus demonstrates the enabling of higher data rate operation for high capacity memory modules - the basic requirement for mitigating the dependency between memory capacity and memory bandwidth.

Implications for System Memory Capacity
One of the primary advantages of the LRDIMM is the ability to dramatically increase total system memory capacity without sacrificing speed. By electrically isolating the DRAM from the data bus, additional ranks of DRAM can be added to each DIMM while maintaining signal integrity, and additional DIMMs can be installed on each system memory channel. LRDIMM capacities up to 32GB are possible today with 4Rx4 modules using 4 Gb, DDP (dual-die package) DRAM. Since each LRDIMM presents a single electrical load to the host, more DIMMs can be installed per channel as well.
Assuming a high capacity server with two processors, three DIMM slots per channel, and four channels per processor, total system memory using LRDIMMs can be increased by two to three times over RDIMM capacity on the same system. Figure 5 shows typical RDIMM and LRDIMM capacity limits for each operating speed and voltage.

<table>
<thead>
<tr>
<th>Speed (MT/s)</th>
<th>Voltage</th>
<th>Maximum density RDIMM</th>
<th>DIMMs per channel</th>
<th>DIMMs per system</th>
<th>System Capacity</th>
<th>Maximum density LRDIMM</th>
<th>DIMMs per channel</th>
<th>DIMMs per system</th>
<th>System Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>1.5V</td>
<td>16 GB, 2Rx4, 4Gb</td>
<td>3</td>
<td>24</td>
<td>364 GB</td>
<td>32 GB, 4Rx4, 4Gb</td>
<td>3</td>
<td>24</td>
<td>768 GB</td>
</tr>
<tr>
<td></td>
<td>1.35V</td>
<td>16 GB, 2Rx4, 4Gb</td>
<td>2</td>
<td>15</td>
<td>256 GB</td>
<td>32 GB, 4Rx4, 4Gb</td>
<td>3</td>
<td>24</td>
<td>768 GB</td>
</tr>
<tr>
<td>1066</td>
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<td>16 GB, 2Rx4, 4Gb</td>
<td>2</td>
<td>15</td>
<td>256 GB</td>
<td>32 GB, 4Rx4, 4Gb</td>
<td>3</td>
<td>24</td>
<td>768 GB</td>
</tr>
<tr>
<td></td>
<td>1.35V</td>
<td>16 GB, 2Rx4, 4Gb</td>
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<td>8</td>
<td>128 GB</td>
<td>32 GB, 4Rx4, 4Gb</td>
<td>2</td>
<td>16</td>
<td>512 GB</td>
</tr>
</tbody>
</table>

**Figure 5: Typical RDIMM and LRDIMM capacity limits for each operating speed and voltage.**

For 1.5V DDR3 operation at 800 MT/s (mega-transfers per second), a system fully populated with RDIMM could reach 384GB, using three 16GB 2Rx4 RDIMMs per channel. With support for 32GB 4Rx4 modules, system memory capacity using LRDIMM can double that limit, reaching 768 GB. System chip-select limits (typically 8 total DRAM ranks per channel) can be overcome using the LRDIMM’s rank multiplication feature, allowing the 12 physical ranks per channel needed in this case.

At higher speeds such as 1066 or 1333 MT/s, signal integrity constraints prevent three DIMM per channel RDIMM configurations. For 1.5V DDR3 operation at 1066 or 1333 MT/s, maximum RDIMM capacity is 256 GB. The LRDIMM does not face the same signal integrity limit, allowing full three DIMM per channel operation at 1066 MT/s (and at 1333 MT/s as a stretch goal), with total system memory capacity remaining at 768 GB, a 3x advantage over RDIMM. For 1.35V DDR3L operation at 1333 MT/s, the LRDIMM advantage is even greater.

**Minimal Incremental Power Impact of LRDIMM**
The LRDIMM not only enables server systems with higher memory capacities, it does so with minimum power penalty. While the memory buffer on a single LRDIMM in a oneDIMM per channel configuration draws more power than the registering clock driver on a single RDIMM in the same configuration, the difference is greatly reduced for higher-density 2 and 3 DIMM per channel configurations, as shown in Figures 6 and 7.

Figure 6 shows the normalized power per RDIMM or LRDIMM for one and two DIMM per channel configurations at various speeds. Since actual power consumed depends primarily on the memory density and DRAM technology used, relative power is shown here for LRDIMMs and RDIMMs using the same generation DRAM on equivalent 4Rx4, 32GB modules. RDIMM module power at 800 MT/s was normalized to 1.00, and other results scaled to that reading. Memory was exercised using an industry-standard benchmarking tool set to generate maximum bandwidth with 50 percent reads and 50 percent writes.
Figure 6: Normalized power per RDIMM or LRDIMM (32GB 4Rx4, Closed Page, 50/50 Read/Write) for one and two DIMM per channel configurations at various speeds.

At 800 MT/s in a one DIMM per channel configuration, LRDIMM power was 17 percent higher than RDIMM power, but at 800 MT/s in a two DIMM per channel configuration, LRDIMM power measured three percent lower than RDIMM power. At 1066 MT/s in a one DIMM per channel configuration, LRDIMM power was 15 percent higher than RDIMM power, but again dropped significantly in a two DIMM per channel configuration, to a level 15 percent below one DIMM per channel RDIMM power. At 1333 MT/s, power per LRDIMM was 28 percent lower at two DIMM per channel than at one DIMM per channel.

Figure 7: Normalized power per DIMM (32GB 4Rx4, Closed Page) for maximum bandwidth memory accesses with 100 percent reads.

Figure 7 shows similar results for maximum bandwidth memory accesses with 100 percent reads. The power differential at one DIMM per channel is slightly higher than in the 50/50 read/write case, but again drops off significantly in two DIMM per channel configurations. Since the LRDIMM is primarily intended for high-density memory applications, power per LRDIMM at 2 DIMM per channel should be of more interest to end-users than power in one DIMM per channel configurations. Figures 6 and 7 demonstrate that for the higher-density two DIMM per channel configurations, end-users enjoy the benefits of LRDIMM with no power penalty.

Improved Power Efficiency at two and three DIMM per Channel

The LRDIMM power efficiency gains at 2 DIMM per channel result from the architectural advantage of having the memory buffer on each LRDIMM located between the memory controller and the DRAM, rather than having all DRAM on all RDIMMs on a given memory channel connected directly to the memory controller. This allows for power-saving termination options for DRAM located on non-target LRDIMMs that are not possible for RDIMMs, and for lower drive strengths due to the
lower number of loads on a given channel. These same advantages extend to three DIMM per channel configurations as well.

Consider the one DIMM per channel Read case shown in Figure 8. For the RDIMM, active DRAM power includes the DQ output driver of the target rank identified as Item 1, and the non-target DRAM termination identified as Item 2. In the one DIMM per channel case, these are similar for the LRDIMM, which adds memory buffer MDQ receiver termination power identified as Item 3, as well as the memory buffer MDQ receiver, DLL, and DQ output driver power identified as Item 4. Items 3 and 4 are additive to the equivalent RDIMM power at one DIMM per channel, which accounts for the higher LRDIMM power in the one DIMM per channel case.

![Figure 8: The power-consuming circuits for the one DIMM per channel read case.](image)

In the two DIMM per channel case shown in Figure 9, the RDIMM system requires additional non-target DRAM terminations on the adjacent RDIMM, labeled as Item 2. In the two DIMM per channel LRDIMM case, the adjacent LRDIMM requires only the additional power needed for the non-target memory buffer DQ termination, labeled as Item 5. By isolating the non-target DRAM from the main memory channel, termination requirements for optimum signal integrity can be modified, and incremental power for additional LRDIMMs can be minimized.
The iMB enables further power optimization by allowing more power-efficient settings for post-buffer ODT (on-die termination) and Ron (on resistance) settings, given the shorter trace lengths and the reduced number of electrical loads between the iMB and the DRAM, compared to the trace lengths from the host memory controller to the DRAM on an RDIMM-based system. In Figure 9, note that the DRAM DQ driver labeled as Item 1 sees seven DRAM loads in addition to the remote host controller in the RDIMM case, while the DRAM DQ driver in the LRDIMM case sees only three DRAM loads and the MB.

A hypothetical example comparing the incremental DC power required by the second RDIMM or LRDIMM in a two DIMM per channel configuration shows the magnitude of the achievable power savings. If the LRDIMM's non-target iMB DQ termination is 60 ohms, termination voltage is 750mV (VDD/2), and the DQ signal level is 1250mV (high) or 250mv (low), power per bit is calculated as follows for the LRDIMM:

$$P = \frac{V^2}{R} = \frac{(1.25 - 0.75)^2}{60} = 4.17 \text{ mW}$$

For the RDIMM, the two non-target DRAM terminations may need to be set to 40 ohms, a parallel combination of 20 ohms, which gives:

$$P = \frac{V^2}{R} = \frac{(1.25 - 0.75)^2}{20} = 12.5 \text{ mW}$$

This would save 8.33 mW per bit for the non-target DIMM, or approximately 900 mW for the 108 bits of the data bus (64 DQ data bits, 8 ECC DQ bits, and 36 DQS strobe bits.)

In addition, dynamic power savings are achievable due to the reduced number of capacitive loads charging or discharging in the LRDIMM 2 DIMM per channel case compared to the RDIMM 2 DIMM per channel case. For each data bit, the DQ driver sees 4 additional loads going from 1 DIMM per channel to 2 DIMM per channel in the RDIMM case, and only 1 additional load in the LRDIMM case. Assuming a 2 pF input capacitance for each of these 3 additional loads toggling at 1333 MHz, with 50% of the inputs charging or discharging for a random data pattern with a high-to-low voltage
swing of 1.0V, the LRDIMM 2 DIMM per channel case could save

\[ P = 3 \times 0.5 \times (V_{\text{RMS}} \times I_{\text{RMS}}) = 1.5 \times (V/\sqrt{2}) \times ((V/\sqrt{2})/Z) = 1.5 \times (V^2/2) \times (2nfC), \]  

or

\[ P = 1.5 \times \pi \times 1.333E9 \times 2E-12 = 12.5 \text{ mW per bit} \]

For the 108 bits of the data bus, total dynamic power savings would be approximately 1350 mW. Combined with the DC power savings calculated above, the LRDIMM 2 DIMM per channel case could save over 2W, a substantial improvement in power efficiency over RDIMM technology in high-density configurations.