Stable pulse generator uses matched transistors in a current mirror

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Using CMOS gates to generate pulses sometimes causes timing uncertainty due to gate-threshold variations. For accurate pulse widths, you can use BJTs (bipolar-junction transistors). Basing the design on current comparison allows the circuits to operate at low voltages. Proper clamping of the timing capacitor avoids pulse shortening with increased repetition frequency. These circuits work with somewhat less accuracy at supply voltages lower than 5V.

The heart of this design is a current mirror using modern dual transistors. Process improvements have made many ordinary dual transistors inherently well-matched. Testing a statistically significant sample of PMBT856 devices typically yields a better-than-1-mV match and no mismatches at voltages greater than 2 mV. As has been true for decades, PNP-transistor pairs are better matched than NPN transistors. Testing PMBT3904 devices yields 2-mV matches, with none worse than 3 mV. The packages measure approximately 2 mm on a side, which gives good thermal coupling between the pair. A current mirror with devices having 2-mV mismatch has 8% error. Devices with 3-mV mismatch yield 12% current error. Even with these errors, the circuit makes pulses that are more predictable than those that CMOS devices make.

Figure 1 depicts a simple implementation of a current-mirror pulse generator. It provides good performance over a 0 to 100°C temperature range (Figure 2). The closely spaced traces in the waveforms of these circuits are the 0 and 100°C outputs. Source V₂ produces a 40-kHz square wave with a 33% duty cycle. The negative transition of this wave produces a peak current of 4 mA in timing capacitor C₁. A time constant of 4.7 μsec is set with the value of resistor R₁. The timing current of C₁ and R₁ passes through diode-connected transistor Q₁, which, being connected in parallel with the base-emitter junction of Q₂, forms a current mirror that replicates in Q₂ the timing current in C₁ and R₁. Because the base-to-emitter-voltage-to-emitter-current curves of Q₁ and Q₂ match and Q₁ and Q₂ are at the same temperature, Q₂ current matches Q₁ current. A quiescent current of about 0.85 mA is set in R₃. When the timing pulse increases Q₂’s current to exceed R₃’s quiescent current, Q₃ lacks base current and turns off, initiating a negative pulse across load resistor R₄.
When the timing current decays below the quiescent current of \( R_3 \), base current flows into \( Q_3 \), turning it on and terminating the pulse on \( R_4 \). \( Q_2 \) saturates early in this pulse and becomes less saturated as the timing current decays.

When \( V_2 \) transitions positive, it drives the bulk of its current into \( D_1 \), yielding a short recovery time constant. \( D_1 \) ceases to conduct at one diode drop above \( V_1 \)'s supply voltage, so the recovery tail from that diode drop to the quiescent base voltage of \( Q_1 \) depends on the current decay in \( R_1 \), which is a longer time constant. This simple circuit is stable, varying less than 4\% over 100°C.

Although stable, this circuit does not provide high-speed operation. In the circuit’s quiescent state, there is no current in either \( Q_1 \) or \( Q_2 \), making for a low gain bandwidth. Also, \( Q_3 \) is in saturation, delaying the initial fall of the pulse across \( R_4 \) because the free carriers must leave the base region. \( Q_2 \) also saturates during the pulse, delaying the rise at the end of the pulse.

**Figure 3** depicts an improved current-mirror pulse generator. In this circuit, the operation of \( C_1 \), \( R_1 \), and \( D_1 \) follows that of **Figure 1**. Changing \( D_1 \) to a Schottky diode reduces the recovery-tail voltage that \( R_1 \) must dissipate. Add \( R_2 \) to draw a keep-alive current of 100 \( \mu \)A through \( Q_1 \) and \( Q_2 \), speeding turn-on. These keep-alive currents need not affect the timing. You can cancel out their effect with a slight reduction in the value of \( R_3 \). Fitting \( Q_3 \) and \( Q_4 \) with Schottky clamps \( D_2 \) and \( D_3 \), respectively, keeps the transistors out of saturation. These changes improve high-speed performance (**Figure 4**).
Although improved, the circuit still relies on $D_1$ for the final tail of recovery. To eliminate this problem, you can replace $D_1$ with a fourth transistor, $Q_4$ (Figure 5). Because transistors $Q_1$ and $Q_2$ are slightly conducting, a voltage one diode drop below that of supply $V_1$ is always present at their bases. You filter this voltage with $R_5$ and $C_2$ and provide it as a bias to the base of $Q_4$. This step keeps $Q_4$ nearer the threshold of conduction than would a diode to supply $V_1$. When source $V_2$ changes to a negative state, $Q_4$ is fully off and draws no current. When $V_2$ changes to a positive state, the emitter of $Q_4$ conducts at voltages above $V_1$ to catch the recovery transition, further reducing the recovery-tail amplitude.

$R_6$ may be used to limit $Q_4$'s base current, but its omission is acceptable if source $V_1$ has sufficient output resistance. It may be destructive to apply source $V_2$ swings large enough to cause excess reverse voltage across the $Q_4$ base-emitter junction. $Q_3$ and $Q_4$ can share the same package. These additions further improve the pulse generator's high-speed performance (Figure 6).