This book collects the best practices FPGA-based Prototyping of SoC and ASIC devices into one place for the first time, drawing upon not only the authors' own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future.

The book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an FPGA-based prototyping project. We start by analyzing the challenges and benefits of FPGA-based Prototyping and how they compare to other prototyping methods. We present the current state of the available FPGA technology and tools and how to get started on a project. The FPMM also compares between home-made and outsourced FPGA platforms and how to analyze which will best meet the needs of a given project. The central chapters deal with implementing an SoC design in FPGA technology including clocking, conversion of memory, partitioning, multiplexing and handling IP amongst many other subjects. The important subject of bringing up the design on the FPGA boards is covered next, including the introduction of the real design into the board, running embedded software upon it in and debugging and iterating in a lab environment. Finally we explore how the FPGA-based Prototype can be linked into other verification methodologies, including RTL simulation and virtual models in SystemC.

Along the way, the reader will discover that an adoption of FPGA-based Prototyping from the beginning of a project, and an approach we call Design-for-Prototyping, will greatly increase the success of the prototype and the whole SoC project, especially the embedded software portion. Design-for-Prototyping is introduced and explained and promoted as a manifesto for better SoC design.

I did a review of this book about a year ago that you can find here.
Chapter listing:
Chapter 1: Introduction: the challenge of system verification
Chapter 2: What can FPGA-based prototyping do for us
Chapter 3: FPGA technology today: chips and tools
Chapter 4: Getting started
Chapter 5: Which platform? (1) build-your own
Chapter 6: Which platform? (2) ready-made
Chapter 7: Getting the design ready for the prototype - Chapter excerpt
Chapter 8: Partitioning and reconnecting
Chapter 9: Design-for-prototyping
Chapter 10: IP and high-speed interfaces
Chapter 11: Bring up and debug: the prototype in the lab
Chapter 12: Breaking out of the lab: the prototype in the field
Chapter 13: Prototyping + Verification = the best of both worlds
Chapter 14: The future of prototyping
Chapter 15: Conclusions

Chapter 7: Getting the design ready for the prototype
This chapter describes the main prototyping challenges, common practices and the process of taking an SoC design into the FPGA-based prototyping system. It covers SoC design-related issues, techniques to make the design prototyping friendly and how to use FPGA special-purpose resources. We cover SoC library cells, memories and clock gating in depth. We also revisit the implementation process and common tools outlined in chapter 3 in order to accomplish the best system performance.

We will be previewing the sections on clock gating.

The principle authors for this segment are Doug Amos and Ramanan Sanjeevi Krishnan of Synopsys.

First segment 7.3 Clock gating
This segment 7.4 Automatic gated-clock conversion

If you want a hard copy of this book, you can get that from here.

Alternatively, if you are willing to answer a bunch of questions about your design and prototyping environment, Synopsys is now making soft versions of the book available for free. Just go here and follow instructions.

Brian Bailey – keeping you covered

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