A dc-blocking capacitor, which you commonly apply in series with each data wire in a differential link, can serve many purposes. It can, for example, shift the average dc-bias level of the signal to adapt logic families using different voltage standards. It can protect the transmitter, the receiver, or both from destructive overload events that can happen due to poor power-up sequencing. It can function as part of a circuit that detects when the lines are disconnected. In all of these applications, the dc-blocking circuit must not distort the data passing through it.

**Figure 1** illustrates a typical electrical model of a dc-blocking capacitor as you might apply it in series with a serial link. The model shows one PCB-trace input and one output. Physically, the capacitor solders onto mounting pads that connect the input and the output traces. Electrically, the figure substitutes for the physical capacitor a schematic comprising the three main elements of the standard electrical model for a capacitor. $C_{\text{BULK}}$ represents the nominal capacitance of the component. $L_{\text{SERIES}}$ is the layout inductance associated with the pads, vias, and any parts of the capacitor body the signal current traverses. $R_{\text{SERIES}}$ is the equivalent series resistance of the component. Figure 1 lists typical values for a garden-variety, EIA 0402-sized, 6.3V capacitor. The figure also includes a fourth element, $C_{\text{BODY}}$. That element represents the parasitic capacitance between the physical capacitor body and all other nearby objects, including the reference planes.
The first step in any circuit analysis involves a quick evaluation of the circuit impedances to see whether you can ignore any elements. Assume a link rate of 6.25 Gbps, for which the frequency of the alternating 101010 pattern, the fastest pattern you can make, equals 3.125 GHz. **Figure 1** lists the impedance magnitudes of the four model elements at that frequency.

The impedances of the bulk capacitance and the series resistance are negligible; the series inductance and parasitic-shunt capacitance are the significant elements. The circuit looks like one short section of a ladder-circuit model for a distributed transmission line. The impedance of the circuit equals

\[ \sqrt{\frac{L_{\text{SERIES}}}{C_{\text{BODY}}}} \]

where \( L_{\text{SERIES}} \) is the series inductance and \( C_{\text{BODY}} \) is the body capacitance.

When a rising edge arrives at the input terminus, if the circuit has too much body capacitance and too little series inductance, the impedance falls below the PCB's trace impedance, and the circuit reflects a brief negative pulse. If, on the other hand, the circuit has too much series inductance and too little body capacitance, so that the impedance exceeds the PCB trace's impedance, the circuit reflects a brief positive pulse. Adjust the inductance and capacitance to the correct ratio, and the circuit becomes almost completely electrically transparent. That is the secret to exceptional blocking-capacitor performance.

One way to lower the body capacitance is to cut a small, round void in the reference-plane layer right under the capacitor, thus relieving the capacitance to ground and slightly increasing the series inductance. Both effects increase the circuit impedance.

An analog engineer may suggest that you intentionally shrink the value of the bulk capacitance until the frequency of the series resonance formed by the bulk capacitance and the series inductance coincides with 3.125 GHz. Unfortunately, tuning the bulk capacitor in that way gains advantage only in one narrow band and still leaves the parasitic body capacitance to create reflections. Enlarging bulk capacitance until its impedance becomes negligible leaves you with only series inductance and body capacitance to consider. You can balance these elements against each other to obtain almost ideal performance.

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