From the Preface:

“Everything should be made as simple as possible, but not simpler.”

—Albert Einstein

Printed circuit-board and IC-package design used to be a field that involved expertise in layout, CAD, logic design, heat transfer, mechanical engineering, and reliability analysis. With modern digital electronic systems pushing beyond the 1-GHz barrier, packaging and board designers must now balance signal integrity and electrical performance with these other concerns.

Everyone who touches the physical design of a product has the potential of affecting the performance. All designers should understand how what they do will affect signal integrity or, at the very least, be able to talk with engineers who are responsible for the signal integrity.

The old design methodology of building prototypes, hoping they work, and then testing them to find out is no longer cost effective when time to market is as important as cost and performance. If signal integrity is not taken into account from the beginning, there is little hope a design will work the first time.

In our new “high-speed” world, where the packaging and interconnect are no longer electrically transparent to the signals, a new methodology for designing a product right the first time is needed. This new methodology is based on predictability. The first step is to use established design guidelines based on engineering discipline. The second step is to evaluate the expected performance by “putting in the numbers.” This is what distinguishes engineering from guesswork. It takes advantage of four important tools: rules of thumb, analytic approximations, numerical simulation tools, and measurements. With an efficient design and simulation process, many of the trade-offs between the expected performance and the ultimate cost can be evaluated early in the design cycle, where the time, risk, and cost savings will have the biggest impact. The way to solve signal integrity problems is to first understand their origin and then apply all the tools in our toolbox to find and verify the optimum solution.

The design process is an intuitive one. The source of inspiration for a new way of solving a problem is that mysterious world of imagination and creativity. An idea is generated and the analytical powers of our technical training take over to massage the idea into a practical solution. Though computer simulations are absolutely necessary for final verification of a solution, they only rarely aid in our intuitive understanding. Rather, it is an understanding of the mechanisms, principles and definitions, and exposure to the possibilities, that contribute to the creation of a solution. Arriving at that initial guess and knowing the places to look for solutions require understanding and
imagination.
This book emphasizes the intuitive approach. It offers a framework for understanding the electrical properties of interconnects and materials that apply across the entire hierarchy from on-chip, through the packages, circuit boards, connectors, and cables.

Those struggling with the confusing and sometimes contradictory statements made in the trade press will use this book as their starting place. Those experienced in electrical design will use this book as the place to finally understand what the equations mean.

The book can be purchased here.

Chapter listing:
Chapter 1. Signal Integrity Is in Your Future
Chapter 2. Time and Frequency Domains
Chapter 3. Impedance and Electrical Models
Chapter 4. The Physical Basis of Resistance
Chapter 5. The Physical Basis of Capacitance
Chapter 6. The Physical Basis of Inductance
Chapter 7. The Physical Basis of Transmission Lines
Chapter 8. Transmission Lines and Reflections
Chapter 10. Cross Talk in Transmission Lines
Chapter 11. Differential Pairs and Differential Impedance
Chapter 12. S-Parameters for Signal Integrity Applications
Chapter 13. The Power Distribution Network (PDN) – Featured Chapter

Appendix A. 100 General Design Guidelines to Minimize Signal-Integrity Problems
Appendix B. 100 Collected Rules of Thumb to Help Estimate Signal-Integrity Effects

Chapter 13. The Power Distribution Network (PDN) – Featured Chapter

The power distribution or delivery network (PDN) consists of all those interconnects from the voltage regulator module (VRM) to the pads on the chip and the metallization on the die that locally distribute power and return current. This includes the VRM itself, the bulk decoupling capacitors, the vias, the traces, the planes on the circuit board, the additional capacitors added to the board, the solder balls or leads of the packages, the interconnects in the packages mounted to the board, the wire bonds or C4 solder balls, and the interconnects on the chips themselves.
The primary difference between the PDN and signal paths is that there is just one net for each voltage rail in the PDN. It can be a very large net that can physically span the entire board and have many components attached.

Note that only the first ¼ of this 100 page chapter will be previewed here.

In this segment
13.1 The Problem
13.2 The Root Cause
13.3 The Most Important Design Guidelines for the PDN
13.4 Establishing the Target Impedance Is Hard

Part 2 contains
13.5 Every Product Has a Unique PDN Requirement
13.6 Engineering the PDN
13.7 The VRM
13.8 Simulating Impedance with SPICE
13.9 On-die Capacitance

The book can be purchased here.

Eric Bogatin received his B.S. in physics from MIT in 1976 and his M.S. and Ph.D. in physics from the University of Arizona in Tucson in 1980. For more than thirty years he has been active in the fields of signal integrity and interconnect design. He worked in senior engineering and management roles at AT&T Bell Labs, Raychem Corp., Sun Microsystems, and Interconnect Devices Inc. Recognizing a need in the industry for quality technical training in signal integrity, he created Bogatin Enterprises, which has grown to be a world-leading provider of signal integrity training services. As a “Signal Integrity Evangelist,” Eric turns complexity into practical design principles, leveraging commercially available analysis techniques and measurement tools.

This posting is part of the EDA Designline power series and is archived and updated. The root is accessible here. Please send me any updates, additions, references, white papers or other materials that should be associated with this posting. Thank you for making this a success - Brian Bailey.