EDA/IP Weekly Roundup - Apr 25th

Brian Bailey - April 25, 2012

This is a roundup of news or activities in the past few days that may be of interest to people. It appears as if I will have to split this into several pieces before long and provide a tools roundup, a research roundup and an IP roundup. Any thoughts?

**Symtavision** has announced that SymTA/S supports the design of ISO 26262 compliant mixed-criticality automotive electronics systems. The SymTA/S methodology overcomes the inherent safety versus efficiency conflicts, especially when ‘freedom from interference’ must be realized between software partitions with different criticality levels. The SymTA/S methodology meets the primary ISO 26262 requirement to provide reliable coverage for failure and error-free scenarios by undertaking timing analyses to optimize and verify the ECU software schedule. Crucial to this is the ability to use SymTA/S timing analyses to select configurations for OS services such as watchdog timeouts and timing protection budgets rather than simply react to timing failures while the target system is running.

Offering a unique opportunity to enter the 49th Design Automation Conference (DAC) for free, **Atrenta, Cadence, and SpringSoft** are jointly sponsoring three-day exhibit passes through the fourth annual ‘I LOVE DAC’ campaign. Attendees who want to take advantage of this offer need to register at www.DAC.com no later than May 15th. DAC is the premier conference devoted to design and design automation of electronic systems. The conference and exhibition will be held at Moscone Center in San Francisco, California, from June 3-7, 2012.

**Mentor Graphics** has announced that Questa Verification IP (VIP) now supports several MIPI Alliance specifications, including CSI, DSI and the recently announced LLI. As a Contributor Member in MIPI Alliance, Mentor sees the standardization of interfaces targeted for use in mobile devices as a step forward for the industry, decreasing time to market, reducing costs and improving interoperability. Questa VIP provides engineers with standard SystemVerilog components for both UVM and OVM using a common architecture for each across all supported protocols. Test plans, compliance tests, test sequences and protocol coverage are all included as SV and XML source code. Questa VIP also includes a comprehensive set of protocol checks, error injection and debug capabilities. When combined with Questa Sim, it allows engineers to quickly trace transactions to signal activity and, vice-versa, debug signals as transactions.

According to **ResearchandMarkets**, the global 3D IC market is expected to grow from $2.21 billion in 2009 to $6.55 billion in 2016 at a CAGR of 16.9% from 2011 to 2016. The companies in this market need to efficiently balance their expenditure between capacity expansion and technology advancement. This is considered critical since the market for 3D ICs is yet to gain complete recognition and its successful penetration into different end-user segments is largely governed by the R&D initiatives. More information [here](#):

**Renesas Electronics** overcame the challenges of the March 2011 Tohoku Pacific coast earthquake
in Japan, that had disrupted key front end fabrication operations, in order to retain a 14 percent market share in the automotive semiconductor market—four percent ahead of its nearest rivals, according to the Strategy Analytics Automotive Electronics service report, “Automotive Semiconductor Vendor 2011 Vendor Market Shares.” The year 2011 brought particularly strong growth in demand for power analog semiconductors. This assisted major power analog semiconductor supplier ST Microelectronics to overtake digital semiconductor biased Freescale. The top five semiconductor vendors for 2011 are now Renesas, Infineon, ST, Freescale, and NXP.

According to analysis from Strategy Analytics, automotive semiconductor vendor annual revenues increased 11 percent to $23 billion in 2011.

The Silicon Integration Initiative will be holding “Si2 Roundup@DAC: Standards in Action” co-located event at the Design Automation Conference. The event will be on Monday, June 4, and will include a celebration of the 10th Anniversary of OpenAccess. This day-long program, consisting of 4 individual events, will showcase activities currently underway with an eye towards demonstrating the value of these programs to the program participants and to the overall semiconductor industry. A featured part of the program will celebrate the 10th Anniversary of OpenAccess. A complimentary luncheon and an afternoon reception will highlight this occasion.

IPextreme has announced a major advance of its Constellations initiative. Constellations is a collective of independent IP companies collaborating at both the marketing and engineering levels. Companies participating in Constellations offer complementary products; membership is open only to non-competing companies to encourage teamwork. Within Constellations, companies work together and share resources to promote mutual success. Constellations member companies currently include Analog Bits, Certus Semiconductor, Northwest Logic, Sonics, Inc., and IPextreme itself. Enrollment is open to new companies at any time, provided that a competitor has not previously secured a place in the program.

Synopsys has released a new Deep Trace Debug feature for users of its HAPS® FPGA-based prototyping systems. With HAPS Deep Trace Debug, prototypers can take advantage of approximately 100 times more signal storage capacity than the traditional memory storage employed by on-chip FPGA logic debuggers. The new Deep Trace Debug feature enhances both capacity and fault isolation capabilities while freeing up the on-chip FPGA memory required for validating complex system-on-chip (SoC) designs.

Brian Bailey – keeping you covered

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