Reduce Mobile Device Costs and Board Area with MIPI Low Latency Interface (LLI) and M-PHY

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Overview:
When designing mobile devices, it is critical to implement technologies that will future-proof your design, minimize BOM costs and board space, and maintain or improve performance. The MIPI Alliance Low Latency Interface (LLI) and M-PHY are two technologies that can help future-proof your design while giving it competitive advantages in terms of cost, board space, performance, and time-to-market.

The webinar will present a case study describing how LLI can be used to minimize DRAM footprint on a mobile phone system board. Particular attention will be paid to real-world implementation issues, such as clock domain, power and voltage management as well as integration with SoC interconnect fabrics.

This webinar will teach you:
- What the LLI and M-PHY technologies are, and best practices for implementation
- How LLI is different than other chip-to-chip interface standards, such as USB and PCIe
- How the LLI point-to-point interconnect can benefit multi-chip systems
- How the LLI controller and M-PHY IP can reduce the silicon footprint on your board
- How LLI can reduce individual BOM and multi-product platform costs

Estimated length: 50 minutes, 10 minutes Q&A

Who should attend:
This webinar is targeted at system architects, mobile device and consumer electronics product managers and designers, design engineers, SoC architects, and project managers.

Presenters:
Hezi Saar, Staff Product Marketing Manager, Synopsys
Hezi Saar serves as a staff product marketing manager at Synopsys and is responsible for its DesignWare MIPI controller and PHY IP product line. He brings more than 17 years of experience in the semiconductor and electronics industries in embedded systems. Prior to joining Synopsys, from 2004 to 2009, Saar served as senior product marketing manager leading Actel's Flash field-programmable-gate-array (FPGA) product lines. Previously, he served as a product marketing manager at ISD/Winbond and as a senior design engineer at RAD Data Communications. Saar holds a bachelor of science degree from Tel Aviv University in computer science and economics and an MBA from Columbia Southern University.
Kurt Shuler, VP of Marketing, Arteris
Kurt Shuler is the VP of marketing at Arteris. He has held senior roles at Intel, Texas Instruments, ARC International and two startups, Virtio and Tenison. Before working in high technology, Kurt flew as an air commando in the U.S. Air Force Special Operations Forces. Kurt earned a B.S. in Aeronautical Engineering from the U.S. Air Force Academy and an MBA from the MIT Sloan School of Management.

Philippe Martin, Vice President, Corporate Applications and Senior Fellow, Arteris
Philippe Martin is Vice President, Corporate Applications and Senior Fellow at Arteris. He has been involved in the development of the MIPI Alliance Low Latency Interface (LLI) specification since the creation of the MIPI Alliance LLI Investigation Group in 2009. Philippe is a renowned expert on LLI and has contributed to the technology through the MIPI Alliance LLI Working Group. Philippe has also participated in the first two commercial implementations by semiconductor companies of the LLI standard.