Semiconductor manufacturers rely on latch-up tests to characterize ICs for susceptibility to electrical failure. Engineers can use various methods to perform latch-up tests, but the only standard that specifies procedures for them—JESD 78 (Ref. 1)—has several limitations. To overcome these limitations, the ESD Association (Rome, NY; www.esda.org) is working on a new test method for CMOS devices called transient latch-up (TLU) testing.

The weaknesses of JESD 78 are varied: The I-test stresses a device's I/O pad structures, but leaves the core circuits untested. The V_{DD} overvoltage test can probe an IC's core, but the voltage you must apply to the device under test (DUT) often destroys the circuit. Some devices tested to the trigger level prescribed in JESD 78 will fail because of electrical overstress (EOS) damage before reaching that level, rendering the test useless.

The TLU tests in the proposed ESD Association standard (SP5.4-2203; Ref. 2) avoid the problems created by JESD 78 because they inject the trigger current into the IC's substrate through a forward-biased diode junction rather than through a reversed-biased junction. To inject current into the DUT, you must pull the power supply (V_{DD}) pin to a negative voltage. Just -1 V or -2 V for 20 µs will inject sufficient current to cause latch-up in susceptible devices while minimizing damage to the DUT. (To learn more about latch-up, see "What is latch-up?")

When you apply a negative voltage to a device's V_{DD} pin, charge carriers flood into the substrate. When the supply voltage returns to normal, the charge carriers rush back out. When charge exits the device through the power-supply pins, it forms a current in the substrate. This current produces localized voltage drops that can cause latch-up. Current flow in the device and voltage drops across
the device's junctions can occur anywhere in the device. Thus, TLU tests increase test coverage and reduce overstress to the device at the same time.

To generate a TLU test pulse, you can use a pulse generator or arbitrary waveform generator. But these instruments lack the output power necessary to create sufficient current in the DUT. A DC+AC signal amplifier drives the DUT during the test.

The amplifier converts the generator's output (typically less than 10 V and less than 100 mA from a 50-Ω source) up to ±30 V and ±3 A from a less than 1-Ω source impedance. The amplifier sums the outputs of the pulse generator and power supply, which produces the test pulse for the DUT. The test setup in Figure 1 lets you generate the TLU test signal, apply it to a device, and monitor the results.

To apply the test signal to a DUT, you need a test fixture. For simple devices, you can build a small, manual test fixture consisting of a device socket, connectors and toggle switches. For more complex devices such as microprocessors and FPGAs, you'll need to use a fixture from an ATE system because you must first apply test vectors to the DUT to get it into a known state before you apply the test pulse.

**Test Procedure**

A complete procedure for performing TLU tests and a flow chart of the steps involved are included in the SP5.4-2003 standard. The steps are outlined below:

1. Connect the device so you can power it and measure the DC or quiescent supply current. To properly bias the DUT's input pins, you may need to use a breadboard, a switch box, or an ATE system.
2. Substitute the transient pulse source—consisting of a pulse generator, signal amplifier, and DC-offset power supply—for one of the power supplies of the device.
3. Power the device to a testable state and measure the supply current.
4. Apply the transient pulse to the supply pins.
5. Observe the voltage and current at the supply pin on an oscilloscope. If the supply current abruptly rises after the disturbance and stays at this elevated level, the DUT may have latched-up.

![Figure 1](image1.png)

Figure 2. The red (upper) trace depicts a device's supply voltage dipping below ground for 20 µs, while the blue (lower) trace indicates the resulting reverse current surge (~900 mA) and higher post-pulse level (200 mA) caused by latch-up.

**Case study**
**Figure 2** shows the results of a test of a mixed-signal telecom IC powered to -3.3 V. We preconditioned the device to a stable and repeatable operating current by setting all of the input pins to logic low.

We connected the transient-pulse source to the DUT's digital supply pins and then applied power to the device. We measured the DUT's quiescent supply current with an oscilloscope using a current probe clipped onto the supply current trace and found negligible supply current (lower trace, point A).

We then subjected the DUT to the transient pulse (upper trace), which produced a disturbance on the $V_{DD}$ voltage trace. After the disturbance ended, the supply current settled to about 200 mA (lower trace, point B).

From operating the DUT prior to the TLU test, we knew that a change in operational state couldn't cause the elevated supply current. Instead, we interpreted the change in quiescent supply current as a latch-up failure. Further electrical testing showed that this TLU failure did not cause EOS or functional defects. Thus, TLU testing is less likely to destroy a device.

**References**