TLP testing gains momentum

Martin Rowe - September 01, 2002

ESD events that damage semiconductor devices come from people, from handlers and sorters, or from a device itself if it obtains sufficient static charge. ESD circuit designers add protection circuits to each pin of a device to increase its immunity to ESD. You must test the protection circuits, called "structures," by subjecting the device under test (DUT) to ESD events—specifying the voltage across a DUT and analyzing when and how the protection circuits fail. When the protection circuits fail, ESD-induced current damages the device.

Standards such as ESD STM5.1-2001 (Ref. 1) require that a device undergo testing with the human-body model (HBM) discharge waveform, and most IC manufacturers specify the highest HBM voltage level a device can withstand. The HBM discharge-current waveform (Figure 1) contains a fast (2 ns to 10 ns) rising edge followed by an exponential decay. While the HBM waveform provides a reasonable simulation of real-world ESD, it has a constantly changing current, which makes taking measurements on a DUT difficult.

![Figure 1](image)

**Figure 1.** A Human Body Model (HBM) pulse rises sharply and then decays exponentially while a TLP pulse holds steady before falling.

A flat-top waveform simplifies voltage and current measurements, because the pulse has a period of little or no change in current. In 1985, two engineers at Intel developed a transmission-line pulse (TLP) testing method that uses a current waveform with a flat amplitude (Ref. 2). IC designers now use TLP testing in increasing numbers, because it provides a reliable, repeatable, and constant-amplitude waveform. TLP testing lets you more accurately measure the conditions that cause IC failures.

Over the last several years, conferences that cover ESD and IC failure analysis have featured
numerous papers on TLP testing, and engineers at many semiconductor manufacturers have built their own TLP testers. Gains in TLP popularity have enticed a few companies to market TLP testers. See "TLP tester manufacturers," p. 38, for more information.

The case for TLP

TLP testing subjects a DUT to a pulsed DC current. Because the test signal has a flat top, the energy dissipated in ESD structures increases linearly throughout the pulse's duration; this differs from an HBM current waveform, which constantly changes amplitude. With a TLP waveform, you can more accurately measure the voltage across and current through a structure and find the voltage and current levels that cause a structure to fail. The TLP waveform doesn't represent any real-world ESD event. It's strictly a tool that designers of ESD protection structures can use to perform circuit analysis and failure analysis. IC designers can use it to analyze how a structure operates before it fails. From the analysis, circuit designers can redesign the protection structures and improve protection.

Because it has a uniform shape, a TLP pulse lets you measure the voltage and current in a DUT over its operating range. If you adjust the width of the TLP waveform, you can adjust its energy to match that of an HBM waveform. That correlation helps you determine the amplitude of the HBM waveform that should cause an ESD protection structure to fail. Typically, ESD circuit designers have used TLP pulses with widths of 75 ns to 200 ns (Ref. 3). The best correlation between energy in a TLP test pulse and that of a 150-ns HBM test pulse occurs with an 80-ns TLP test pulse width. The ESD industry, however, has settled on a 100-ns pulse width as the de facto standard.

In addition to its width, a pulse's rise time plays a role in how a structure performs. HBM test standards specify an initial rise time between 2 ns and 10 ns. Such a large range leads to a need for selecting the rise time of a TLP test pulse. As part of an analysis of a device's ESD-protection structures, TLP testing may include testing with rise times comparable to those required for HBM tests. But designers should test their structures under harsher conditions than those required by standards. As a result, IC designers often use 200-ps rise time TLP pulses.

Waveform production

To produce a TLP waveform, a TLP tester charges a transmission line with a high-voltage DC source. When the transmission line discharges, the pulse it creates injects current into the DUT.

The original TLP tester designed by Intel's engineers injected a constant current into the DUT for the length of the pulse. Figure 2 shows a system diagram of a constant-current TLP tester. A 50-Ω resistor provides a known, controlled load for the transmission line. A resistor in series with the DUT converts the voltage from the transmission line into a somewhat constant current before injecting it into the DUT.

Figure 2. A constant-current TLP tester uses a resistor to convert voltage from the transmission line into current that flows into the DUT.
A constant-current TLP tester can deliver up to about 4 A to the DUT, but many IC designs require more current. To obtain more current, some engineers use a constant-impedance TLP tester. The constant-impedance TLP tester in Figure 3 can deliver up to 10 A. In this type of tester, an attenuator adjusts the voltage level that the DUT receives and also prevents signals from the DUT from reflecting off the transmission line and returning to the DUT as extra energy. Reflections distort waveforms, which reduces accuracy of the measurements. Low-pass filters alter the pulse's rise time, typically over a range of 0.2 ns to 10 ns.

![Figure 3. A constant-impedance TLP tester keeps the impedance constant through the test circuit, which controls the current through the DUT.](image)

TLP testers, whether purchased or built in-house, use a 50-Ω coaxial cable, the length of which sets the test pulse's length. Each foot of cable adds roughly 3 ns to the pulse, so to get a 100-ns pulse you need about 33 ft of cable. A low-resistance relay connects the cable to the DUT either through a resistor (constant-current method) or an attenuator and low-pass filter (constant-impedance method).

To measure the voltage across and the current through a DUT during a TLP pulse, a TLP tester uses an oscilloscope with at least a 500-MHz bandwidth. A voltage probe connects between the DUT's test pin and ground. A current probe measures the current that enters the DUT.

While many TLP testers use constant-current and constant-impedance methods to calculate current, others use a different technique: time-domain reflectometry. These testers use a delay line and an attenuator following the relay. The tester measures the amplitude of the current pulse entering the delay line, and then it measures the amplitude of the reflection from the DUT. From the difference in amplitude, the tester can calculate the current and voltage in the DUT. The delay line ensures that the reflected signal won't interfere with measurements on the incident signal.

Regardless of which method you use to calculate current, the TLP tester injects current into a MOS device's drain with the gate and source grounded. As the tester increases the pulse amplitude, failures will begin to occur when the end of the pulse reaches the DUT. By that time, the device will have had to withstand all of the pulse's total energy.

**TLP measurements**
Breakdown occurs when the leakage current suddenly increases, which usually occurs at point \( I_{t2} \) (the second snapback point) of a device’s I-V curve. A TLP tester must build an I-V curve through numerous sets of measurements. Figure 4 shows a typical I-V curve (blue trace) and leakage current (red trace) of an ESD protection structure. For each point on the curve, the tester applies a TLP pulse to the ESD protection structure under test while the device is unpowered (Figure 5a). The oscilloscope triggers on the pulse's rising edge and makes voltage and current measurements in the 70% to 90% range of the test pulse's width, which ensures a stable current flow at the time of measurement.

After measuring a point in the DUT's I-V curve, the tester must check for damage by measuring the leakage current at the pins under test. Depending on the structure design, the TLP tester may also need to apply power to the DUT's \( V_{cc} \) and ground pins (Figure 5b). Then the tester connects the test pin to a DC voltage source set to a voltage level that the device sees during normal operation. After the tester measures the leakage current in the test pin, it adds that point to the plot in Figure 4. Testing takes about 5 s to 10 s for each point.

The curves in Figure 4 indicate that as voltage across the DUT increases, the I-V curve remains at zero until the structure reaches a turn-on threshold. At that point, the voltage "snaps back" as current increases (point \( V_{t1} \)). As the voltage increases again, the current through the DUT also increases, but the DUT's leakage current remains stable at less than 1 nA. Device failure here occurs at the point just before the second snapback point, \( I_{t2} \), where leakage current jumps to over 1 µA, a jump of about three orders of magnitude. When this "hard failure" occurs, the device will cease to
In some devices, the leakage current may suddenly increase and then return to the level it was at before the sudden increase. Then, as test voltage increases, the device's leakage current will gradually increase to failure levels rather than holding relatively constant until reaching breakdown. Such a condition is called a "soft failure" because the device's protection structures partially recover and the device continues to operate until higher stress levels cause it to permanently fail (Ref. 4).

Some devices can show a sharp increase in leakage current without a second snapback occurring (Ref. 5). Therefore, you can't rely solely on an I-V curve to find the point where breakdown occurs. You must also measure leakage current.

Because a TLP test requires the use of test pulses of increasing current until failure occurs, the DUT will take numerous hits as a tester builds an I-V curve. Engineers at IMEC (Leuven, Belgium) performed measurements with 1000 TLP hits that produced current at levels from 75% of \( I_{t2} \) to 110% of \( I_{t2} \) (Ref. 6). When the test voltage produced current levels at 95% of \( I_{t2} \), the DUT didn't fail, even after 1000 hits.

Tests such as the one at IMEC show that IC designers and ESD engineers have much to learn about TLP testing. Experiments on ICs undergoing stress from TLP tests continues, and the 2002 EOS/ESD Symposium in Charlotte, NC, will feature papers on ESD testing of semiconductor devices. The symposium also will feature a TLP testing tutorial presented by Leo G. Henry of Ion Systems (San Rafael, CA) and a technical session with two papers on TLP testing. (For more information about the symposium, visit [www.esda.org](http://www.esda.org).)

Although 17 years old, TLP testing continues to evolve. Besides understanding the effects of TLP testing on semiconductors, ESD engineers must resolve discrepancies between HBM pulses and TLP pulses if TLP is ever to replace HBM as a standard test. In addition, the industry needs a standard calibration procedure for TLP testers, which will compensate for differences in construction and make test results from one tester comparable to results from others.

*The following company information appeared in the original print version of this article. For up-to-date information about companies, visit the ESD Control/Protection portion of our Buyer's Guide.*

### TLP tester manufacturers

The following companies manufacture test systems that perform ESD testing by generating transmission-line pulses.

<table>
<thead>
<tr>
<th>Company</th>
<th>Address</th>
<th>Phone Number</th>
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<tr>
<td>Barth Electronics</td>
<td>Boulder City, NV</td>
<td>702-293-1576</td>
<td><a href="http://www.barthelectronics.com">www.barthelectronics.com</a></td>
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<td>Oryx Instruments</td>
<td>Fremont, CA</td>
<td>510-249-6320</td>
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<tr>
<td>Thermo Keytek</td>
<td>Lowell, MA</td>
<td>978-275-0800</td>
<td><a href="http://www.thermokeytek.com">www.thermokeytek.com</a></td>
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### References


