Beware ATE Effects When Testing High-Speed ADCs

Fang Xu - June 01, 1999
Fang Xu, Ph.D., is a senior application engineer in Teradyne’s Fast Converter Test Expert Team. He is a member of the team’s Test Assistance Group. He alternates between Paris and Boston.

An intelligent noise-calibration technique can overcome this limitation. To implement this technique, our test program ... as a reference—digitizing the same signal 100 times and generating an averaged spectrum free from run-to-run noise.

$$\text{NOEB} = \frac{\text{SINAD} - 10\log_{10}1.5}{10\log_{10}4}$$

Of these four groups of tests, the SINAD, THD, SNR, NOEB and SFDR test set (predominantly dynamic in nature) showed the least variability in results for the complete suite of tests. If you would like to see the complete results, please send me an e-mail.

To accurately measure the last three (DUT-generated) noise characteristics, we built a test system (Noiserms = intrinsic rms thermal noise of the device input. e = average DNL of the ADC, and

where

These six tester and DUT noise sources contribute to SNR as shown in

To measure the signal-to-noise ratio (SNR) accurately, you must generate the most perfect test signal possible, and then measure SINAD, THD, SFDR and NOEB. However, the test signal is often degraded in a number of ways:

Noise Factors During Testing

Some of these factors are controlled by the test system itself. The issues that can be controlled are:

- Input-pin continuity tests
- Pin open-short tests
- DUT digital-driver-level tests
- Clock-level tests

They are evaluated in a component test at the VHF instruments. Because these factors are not controlled in customer testing, these tests must be performed in the lab (Fig. 2).


differential gain and phase tests; and

SINAD, THD, SNR, NOEB and SFDR tests; and

noise calibration to separate device input circuitry noise and remaining noise inside the filter bandwidth. (For a further explanation of how we modified our tester, see "Optimizing Test Hardware Performance,"

A test head, containing electronic circuits that condition the test signal and which need to be very close to the DUT. (A test head is an electronic interface between the DUT and the test equipment.)

a 5-in. circular PCB, for mounting the test socket and other sensitive components connected to the DUT;

power-supply sources, which provided power to the DUT and also were used to measure DUT power consumption.

high-speed digital channels, for capturing the device's digital output, differential gain and phase programming, pin open-short tests, DUT digital-driver-level tests, and clock-level tests; and

When performing the input-pin continuity test and the differential gain and phase measurement, DC instruments and the tester's VHF instruments are used. Yet, if you are testing a high-speed ADC, you might also want to test:

- Throughput tests
- Noise transfer tests
- Intermodulation distortion tests.

In bench testing, you can employ one set of instruments to measure one parameter and then decide to use another set of instruments to measure another parameter. However, in production testing, this is not possible. In production testing, the extra interface circuit needed for this test will compromise the noise performance.

As the frequency of ADCs increases, the challenge of evaluating the performance of devices in production-scale quantities becomes more difficult. In most cases, the test signals are sent from the tester directly to the DUT. Therefore, the tester and DUT have to be configured in the same way that they would be configured in production. However, if you are testing a high-speed ADC, you can't possibly test all of the parameters in production.

Instead of using relays, the LC channel-separation tree routes a sine wave of a specific frequency directly to the filter inputs. The filter outputs are connected through low-capacitance relays so they can be tied together to simplify the circuit.—Fang Xu

This ADC test interface can evaluate ADC parameters such as noise, offset, linearity, and distortion.

To optimize test-system performance when testing fast ADCs, we made the following modifications to components found on either the 5-in. circular PCB or on the device interface:

- A jumper inside the test head that provides an alternative channel of test input when conventional channels are not available.

- A new VHF interface circuit that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.

- A new power-supply circuit that provides a test interface that is independent of the test head.

- A new clock circuit that provides a test interface that is independent of the test head.

- A new digital output interface circuit that provides a test interface that is independent of the test head.

- A new jitter reduction module that provides a test interface that is independent of the test head.

- A new high-speed digital channel that provides a test interface that is independent of the test head.