Beware ATE Effects When Testing High-Speed ADCs

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The number of effective bits (NOEB) can be calculated from SINAD as follows:

\[
\text{NOEB} = \frac{\text{SINAD} - 10\log_{10}1.5}{10\log_{10}4} + \text{harmonics}
\]

With the device clock running around 41-MHz, we performed the SINAD, THD, SNR, NOEB, and SFDR tests using two different bandpass filters to produce as perfect a test signal as possible. A Fourier analysis of the DUT digitized sine wave (as shown in Figure 2) provided information on the fundamental power as well as on the harmonics and noise. If you minimize these test-system-generated noise sources, you can more accurately measure the noise sources associated with the DUT itself.

We also employed a device interface comprising the following components:

- **Programmable filter module**
- **Jitter reduction module**
- **Power-supply sources**, which provided power to the DUT and also were used to measure DUT power consumption.
- **An ADC's digital outputs have limited current-driving capability, and uncontrolled output source or sink currents can cause problems.**

For further improvement, I developed a jitter reduction module (patent-pending), which we combined with the previous enhancement. The module reduced the relative rms jitter of the clock signal by 30% to as much as 85%. Despite the module's fixed frequency, the clock frequency may be adjusted by changing the divider ratio. The module is described in a patent application filed in May, 2003, U.S. Patent Application 10/554,583.

**Software Enhancements on the Device Interface Board**

To optimize test-system performance when testing fast ADCs, we made the following modifications to components found on either the 5-in. circular PCB or on the device interface:

- When performing the input-pin continuity test and the differential gain and phase measurement, DC instruments and AC instruments are connected in parallel. We enhanced isolation by inserting a relay in series with the LC network to minimize cross talk and effectively reduce the test equipment's capacitive load on the DUT.

The following sections present a more detailed description of the improvements we made to the LC channel-separation tree.