Numerous challenges have to be overcome during design and production of ICs below 90 nm. Manufacturing processes are still being characterized, and the interactions between the physical processes and design features can be extremely subtle and difficult to identify. As a result, meeting yield goals is a bigger challenge than it was at larger technology nodes, and this has a direct impact on profits. The faster a new design can be ramped up to volume production rates, the faster the time to profit (Figure 1).

![Figure 1. As this yield ramp shows, the faster a new design can be ramped up to volume production rates, the faster the time to profit.](image)

Yield management has traditionally been the responsibility of one or more engineers who also are responsible for design, test, production, or processing. Once a design is in production, the yield manager’s job is to make the product “yield better” by, among other things, identifying yield limiters and specifying changes to the design, test, or manufacturing process. Finding the root cause of yield-limiting defects often requires engineers to sort through a large amount of information from many different sources, a process that can take months.

A yield manager usually depends on manufacturing process data such as parametric measurements and in-line inspection data when making an analysis. From the performance history of the manufacturing equipment, the yield manager can see which machines have recurring maintenance issues. Electrical scribe-line tests also can provide an early indication that process variations are starting to drift more than expected.

During wafer sort, test sets or patterns generated using ATPG (automatic test pattern generation) software are applied to the die on ATE (automated test equipment). At this point, the yield manager often uses a spreadsheet to plot the cumulative errors from many wafers into a single wafer map.
that helps identify a failure “signature.”

The yield manager then selects a set of die that most likely contain the yield-limiting defect and sends them to the failure-analysis lab for more detailed analysis. The die-selection criterion is often at a very gross resolution, and it’s common for many (100 or more) die to be sent for further analysis.

In the failure-analysis lab, the engineers verify the failure for each die on a functional tester to ensure the failure’s electrical signature can be duplicated. Then, an engineer attempts to localize the defect to a small block of circuitry and functionally and logically locate the defect in the failing circuit.

Physical fault isolation is the next step the engineers perform, using tools and techniques such as scanning electron microscopes, voltage contrast, and micro- or nano-electrical probing. They physically deprocess the part and then section it to identify the root cause of the yield-limiting defect. Once the cause has been identified, the manufacturer can finally take corrective action, whether it is to change the design, library, or manufacturing process.

**Roadblocks in the yield-management system**

For well-characterized processes such as those for feature sizes of 90 nm and greater, designers usually can be sure that their designs will provide acceptable yield when they follow foundry-supplied DRCs (design rule checks). Yield limiters are typically caused by the manufacturing process and are easy to identify, so 90-nm designs tend to ramp to volume quickly. Expected manufacturing variability that may cause defects is taken into account within the DRC.

At designs nodes below 90 nm, however, yield-limiting defects can be design- or feature-related and are harder to identify. Because the manufacturing processes for these designs are not as mature, unexpected interactions between design features and manufacturing variability are causing an increase in yield-limiting defects. And these often appear to be randomly distributed across the wafer and across lots, making it difficult for the yield manager to identify which devices are affected by systematic issues.

**Figure 2.** Mature yields (that have been in production for as long as 12 to 18 months) decrease an average of 5% for each technology node.

In addition, at very small feature sizes, little real margin exists between the design rules and manufacturing process variations, leading to an average 5% decrease in expected yield with each successively smaller design node for mature products that have been in production for as long as 12 to 18 months (Figure 2). Optical resolution also has become an issue with smaller feature sizes and more metal layers. It’s becoming increasingly difficult to visually identify an issue based on analysis...
of test signatures and manufacturing data alone without the netlist.

To complicate things further, the yield manager may not have access to manufacturing equipment data, the results of optical inspection tests, or wafer-position data. In this situation, the manager has to determine the root cause of systematic yield-limiting defects without all of the data that traditionally has been available. The yield-analysis engineers may need additional time, effort, and money to identify and locate defects with this limited data set.

**Automated diagnosis provides a better roadmap**

One way to improve the time to yield for advanced ICs is by using a diagnosis-driven yield-analysis process that enables the yield manager to make better use of manufacturing test results to find out why and where failures occur. Instead of relying solely on pass/fail information from manufacturing test, the yield manager can take advantage of commercial logic-diagnosis software tools that provide detailed data from the manufacturing test—not just which test pattern failed, but exactly which ones out of millions of cycles failed and for what pins. Engineers can use this detailed information to determine exactly what the defect is and where it occurs. And some vendors provide logic-diagnosis software that is compatible with their on-chip compression software, so the yield manager doesn’t have to decipher compressed data (Ref. 1). The manager can have the software generate diagnosis reports for each failed die, which can then be used to group the die based on matching of specific failures, such as bridges, opens, cell, and metal layers.

At Mentor, our logic-diagnosis software can automatically diagnose large amounts of failures after wafer sort at the same time that manufacturing test is running, which means the yield manager doesn’t have to wait until test is finished for the data to be available. When a die fails a test, the failure log can be sent immediately to a database that also includes diagnosis results. The yield manager can generate a report for each die that specifies the most likely cause of the failure.

In addition, the logic-diagnosis tools can perform diagnosis based on the design and physical layout data, not just on the manufacturing test set. By incorporating the layout information, the tools determine the type of defect and localize it down to its physical coordinates much more quickly than can be done manually, giving the yield manager a head start on identifying defect types and which pin, cell, net, or group of nets may be causing the test failure.

![Figure 3](image.png)

*Figure 3.* A wafer map that shows all failures can hide root causes in the "noise" (left). A map of failing die due to one failure mechanism (right) helps with diagnosis.

For logic-diagnosis software to be useful in ramping yield, the yield manager must be able to analyze the diagnosis results and differentiate systematic defects from random ones. The manager can
generally accomplish this by performing a statistical analysis after diagnosing a large number of failing devices. For instance, after diagnosing the test failures, the yield manager may find that many parts have a bridge defect in the same location. Statistical analysis may help determine that, while several types of defects are randomly distributed across the wafer, this particular defect only occurs in the center of the wafer—indicating a systematic issue. Figure 3 shows how systematic problems can be extracted from the “noise” in a stacked wafer map.

Figure 3 shows how systematic problems can be extracted from the “noise” in a stacked wafer map.

Figure 4. A yield-analysis tool can allow yield managers to specify wafer zones for analysis.

To make the yield manager’s job easier, a yield-analysis methodology that includes statistical analysis that displays different failures mapped across wafers, lots, scan chains, and the die can be used. This methodology allows the yield engineer to see if specific defect mechanisms are evenly distributed, or if there is a correlation with a specific type of defect and a specific part of the die.

Yield-analysis software can indicate a systematic defect as

- the aggregation of a failed feature,
- the difference between the expected and actual failure probability of a failed feature, and
- a group of failed features that is sensitive to certain regions of a stacked wafer map.

With this yield-analysis methodology, the yield manager can analyze a “zone” or area of the wafer (Figure 4) for failure characterization. Using this method, a full analysis could be performed without prior selection. Yield-analysis software tools can then automatically analyze the preselected population according to the zone and display the failure signatures and instances of a particular feature failure (Figure 5, at end of article). The features with the highest probability of systematic defects are displayed with a Pareto chart (Figure 6). The software then allows the yield manager to drill down into the data and see which die on the wafers match a failure signature.

Figure 5. A Pareto chart highlights the occurrence of systematic defects per wafer zone.

Failures are categorized in a way familiar to the yield manager, such as by scan chain number, test
pattern number, scan cell, net name, metal layer, and diagnosis type. Examples of diagnosis types are cell-internal failure, open, bridge, and slow-to-rise.

The tool then creates and displays a stacked wafer map based on the analysis filter selected by the yield manager, whether the results are from one wafer or hundreds of wafers. Systemic failures that occur in a non-evenly distributed fashion across wafer zones become obvious. The die locations that show defects occurring most often within the population are highlighted, so the most likely candidate is even more obvious. Then, the yield manager can produce a report generated by the software that pinpoints the defect’s exact location and describes the failure.

Using an automated system to perform these tasks helps the yield manager more accurately narrow down the defect to a small number of die that can be sent to the failure-analysis lab for further investigation. Along with the die, the manager can supply the lab with detailed information about where to look and what to look for to speed up the process of discovering and verifying the root cause of a yield-limiting defect.

**Identifying an open net**

![Figure 7](image)

*Figure 7. The physical-failure-analysis process on eight selected dies isolated a defect to a malformed layer 2 via, which was leading to an open net.*

Several semiconductor companies were able to benefit from our diagnosis-driven yield-analysis methodology. In one example, a customer had one wafer excursion on a 10-million-gate design at 90 nm. Out of 209 scan fails, diagnosis showed that just over half of the die on the wafer exhibited a defect due to an open defect mechanism. The customer concluded that the cause of the yield excursion was most likely an abnormality in a process step related to the fabrication of single vias in layer 2.

To validate that conclusion, the customer selected eight failing die and performed detailed physical failure analysis on the defects. These die were selected using diagnosis results from wafer-probe testing. The failure-analysis process on all eight dies isolated the defect to a malformed layer 2 via that was leading to an open net in the device (*Figure 7*). The failure-analysis information can also be used to identify and correct the deviant process step to restore the yield back to normal levels (Ref. 2).

**Enhancing yield for a new SOC**

In another example, a manufacturer performed a logic diagnosis on 20 scan fails during preproduction, and the results narrowed down the scan chain failures to one suspect that should be either stuck-at-1 or stuck-at-0, a hard defect in silicon. Three devices were sent to the failure-analysis lab with a diagnostic report that indicated the scan input path that was a suspect as well as
the scan cell. The results of the physical failure analysis were inconclusive and indicated that the defect could be random or was randomly distributed on the die.

When the manufacturer used the diagnosis-driven yield-analysis flow, however, filtered wafer maps showed that there was a higher percentage of scan chain failures in the edge of the wafer than at the center. The exact fault location in the scan chain failing units was isolated. The failure analysis showed poor copper fill, and the process steps were enhanced for all the metal layers. As a result, the manufacturer reduced scan chain failures from 13% to 3%, increasing the yield by 10%. Using diagnosis and physical failure analysis on what appeared to be randomly distributed chain defects helped improve the total yield (Ref. 3).

References

**Figure 5.**

**Figure 5.** With diagnosis-driven yield-analysis tools, manufacturers can analyze a feature type (a bridge, in this example) in a particular zone of a wafer, and the software can then display the failure signatures and instances of a systematic issue.