Coherent clocking speed ADC tests

Mike Curtin - March 01, 2001

When evaluating ADCs, you can duplicate the performance of the coherent test setups of expensive benchtop testers by using a synthesizer within a phase locked loop (PLL). Such a system can achieve sample rates well in excess of 10 MHz. The PLL clock performance is sufficient for 14-bit systems running at a sampling rate of 140 kHz.

A coherent system differs from real-world sampled-data systems, which are generally noncoherent. For noncoherent systems, you don’t know the relationship between the sampled signal’s frequency and the system’s sampling rate. In the lab (or on the production test floor), however, you can control that relationship. For device-test applications, coherent systems offer advantages in two key areas:

- **Antialias filtering.** Designers of sampled-data systems choose a sampling rate that obeys the Nyquist criterion with respect to input bandwidth specifications. If, however, the system sees input signals or noise that exceeds half the sampling rate, the sampling process will introduce into the passband erroneous alias signals that you cannot distinguish from the signal of interest. Most systems employ an antialias filter in front of the system’s ADC to eliminate significant aliasing. Because you have full control of sampling and input frequencies in a coherent system, coherent systems don’t require antialiasing filters.

- **Window-weighting**. In the digital domain, you’ll often want to perform a fast Fourier transform (FFT), which determines an input signal’s energy content with respect to frequency. For ADC tests, further calculations on FFT results provide such specs as signal-to-noise ratio (SNR) and total harmonic distortion (THD). In real-world sampled systems, however, you can’t directly perform an FFT on sampled data and expect accurate results. That’s because any sampled-data system builds up a continuous-time model of the sampled signal for analysis. Such models are finite in length and contain discontinuities; to compensate for these discontinuities, a noncoherent system must multiply the sampled data by a window-weighting function before performing an FFT.

In a coherent system, you control the relationship between the input stimulus and the ADC’s sampling clock, allowing you to exercise as many different codes in the ADC as possible while preventing discontinuities in the captured waveform. Thus, there is no need to apply a window-weighting function when doing an FFT on coherent data. In a coherent sampling system, all the power from the signal and its harmonics will fall into predictable frequency bins, making it easier to measure SNR and THD.
In a coherent sampling system, the following equation defines the relationship between the sampling frequency and the input frequency:

\[ N \times F_{\text{IN}} = M \times F_s \]

or

\[ F_s = \frac{F_{\text{IN}} \times N}{M} \]

where

- \( F_{\text{IN}} \) is the input frequency of the ADC,
- \( F_s \) is the sampling frequency of the ADC,
- \( N \) is the number of points to be sampled for the FFT (2048, for example), and
- \( M \) is an integer number that has no common factors with \( N \).

**Clock generation**

Normally, you could use an integrated test system to generate the clocks required for a coherent sampling system. Although this might be satisfactory in a production environment, it can be too expensive for smaller-scale projects. A simple alternative is to use a PLL to generate the required signals (Figure 1), but it must be flexible enough to handle all the possible combinations of input-signal frequency and sampling rate.

By using one side of the synthesizer plus a loop filter and a VCO as a conventional PLL, and using just the \( N \) divider of the other side, you can program the output frequency so it is coherent with respect to the input signal. Figure 2 shows a practical implementation of this approach. The ADF4213 is a dual-frequency synthesizer that has a 3-GHz RF bandwidth and a 1-GHz IF bandwidth. Here, the RF side of the synthesizer generates a high frequency, 532-MHz signal. The RF output is also applied to the \( N \)-divider for the IF side. The \( N \)-divider output is available on the MUXOUT pin, whose frequency is...
Notice the similarity between this equation and the one shown earlier for a coherent sampling system.

\[
F_S = \frac{R_2 \times N_1}{R_1 \times N_2}
\]

To determine the sampling frequency, \(F_S\), needed for a coherent sampling system, first consider hardware limitations. The AD7894, representing the DUT in this example, is a 14-bit, 5-µs ADC in an eight-lead SOIC package. Allowing for the sample-and-hold acquisition time and the interrupt response time of the data-gathering processor, the maximum sampling rate is 140 kHz. Thus, the coherent sampling frequency should be close to, but less than, 140 kHz.

The VCO imposes a second limit. In this example, the VCO has an output frequency range of 525 to 555 MHz when driven with a tuning voltage of 1 to 4 V. You must ensure the resulting output frequency is within the range of programmed values for R1 and N1.
The AD7894 ADC under test requires a low-going pulse at least 40-ns wide on its CONVST input (lower trace). Inversion of Figure 2’s MUXOUT output (upper trace) provides such a signal.

Figure 3.

A coherent-clock sampling system samples the input over a large, prime number of periods, using the sampled data to build up a continuous time picture. In this example, the input frequency is 10 kHz, and the AD7894 system will take 2048 samples in 149 periods of the input signal. In this case, the value of \(F_s\) comes out at 137.45 kHz. You can achieve this \(F_s\) using the circuit of Figure 2 by setting \(R_1\) to 2 and \(N_1\) to 106496, giving an output from the VCO of 532.48 MHz. This signal feeds back to the RF\(_{IN}\) pin of the ADF4213 and also to the IF\(_{IN}\) pin. With \(N_2\) set to 3874, the output frequency becomes 137.45 kHz.

The PLL supports a 5-kHz phase-frequency-detector (PFD) frequency, a 1-kHz loop bandwidth, and 45° phase margin. In general, this system will work with many VCO output frequency ranges; wider output-frequency ranges will make the scheme more versatile for handling different input signal frequencies.

The AD7894 needs a low-going pulse with a minimum duration of at least 40 ns to drive its CONVST (conversion-start) input. Since the output from the ADF4213 is a high-going pulse, it must be inverted before applying it to the AD7894. Figure 3 shows these waveforms. The active edge in the ADF4213 is the positive-going edge. This means that the active edge going to the AD7894 is the negative-going edge. The negative-going edge triggers the input sample-and-hold, so its jitter determines the overall performance of the ADC.

Controlling pulse width

The ADF4213’s N-counter includes a prescaler and an AB-counter (Figure 4). The prescaler is programmable to values of 8/9 (that is, 8 or 9), 16/17, 32/33, or 64/65. When set to 8/9, the prescaler divides by 8 when its control input is low and by 9 otherwise. With the counters internally connected as in Figure 4, the frequency delivered to the CMOS section is RF\(_{IN}\)/8 with the 8/9 prescaler value programmed over the device’s serial interface bus. The CMOS counter is a classical divide-by-N. It will provide a pulse of duration 8/RF\(_{IN}\) (input frequency to the CMOS counter for 8/9 prescaler setting) every N cycles of the RF\(_{IN}\) (N = BP + A).

For example, with the RFIN set at 532 MHz and the prescaler set to 8/9, the AB counter input frequency is 66.5 MHz, and the resultant output pulse width is 15 ns. That’s not wide enough for the AD7894. But by choosing the maximum prescaler setting of 64/65, the output pulse width becomes 120 ns—more than adequate for the AD7894.
Figure 5. You might need a differential line driver with transformer if your DUT is remote from your synthesizer’s MUXOUT output.

Figure 2 shows an inverter as the drive element for the sampling clock, FS. If the ADC is not close to the MUXOUT pin of the ADF4213, a line driver may be preferable to the inverter. Figure 5 shows one option, the AD8131 differential line driver. Matching is accomplished by using a 100-V resistor in the transformer secondary and two 50-V resistors in series with the AD8131 outputs.

Test results

The FFT obtained, when using the circuit of Figure 2, is shown in Figure 6. The SNR performance gained is 79.6 dB, excluding harmonics, and 79.4 dB with harmonics included. This is comfortably inside the 78-dB specification for the device.

In Figure 6, it is easy to identify the magnitude of the harmonics. The second harmonic is clearly visible at –95 dB, the third harmonic is in the noise floor (–105 dB), the fourth is at a level of –97 dB, the fifth is at –105 dB, and the sixth is at –103 dB. The specification for peak harmonic or spurious signal is –92 dB, and you can see that this is met. The THD specification for the device is –86 dB. You can obtain this value by doing an rms summation of the second to the sixth harmonics. Using the above numbers, you can calculate a THD figure of –92 dB, well inside the published specification.
Figure 7. The FFT for a noncoherent sampling system shows each harmonic’s power distributed among different frequency bins. The inset provides a close-up of the second harmonic’s distribution among frequency bins.

It is worth comparing the coherent-system FFT with the typical result from a noncoherent system. Figure 7 shows the results from a noncoherent system, where $F_s$ is 137 kHz, but the input signal and the sampling signal are not locked. To compensate for the unlocked signal, we applied a Blackman-Harris Window to the sampled data before performing the FFT. Figure 7 makes it immediately obvious that the power of the fundamental and the harmonics is no longer confined to one bin. Instead, each occupies at least three bins, making the determination of harmonics more difficult than in the coherent case. T&MW

For more information

“5 V, 14-Bit Serial, 5 µs ADC in SO-8 Package,” AD7894 data sheet, Analog Devices, Norwood, MA. 1998. [link to PDF]. Editor’s Note 10/24/03: This page has moved: [URL moved].

“Dual RF/IF PLL Frequency Synthesizers,” ADF4210/1/2/3 data sheet. Analog Devices, Norwood, MA. 2000. [link to PDF]. Editor’s Note 10/24/03: This page has moved.


“Low-Cost, High-Speed Differential Driver,” AD8131 data sheet, Analog Devices, Norwood, MA. 2000. [link to PDF]. Editor’s Note 10/24/03: This page has moved.

Travis, Bill, “Remystifying ADCs,” EDN, October 9, 1997. [link to article].

Acknowledgement
The authors would like to thank Declan Carey, who built and tested the circuits presented in this article.

**Mike Curtin**

is applications manager of Analog Devices’ RF and Wireless Components Group in Limerick, Ireland. **Ken Kavanagh** is an applications engineer at Analog Devices in Limerick, Ireland.