Hierarchical test access has become increasingly important with the emergence of System-On-Chip (SOC) technology, which lends itself to test pattern re-use at the device level, board level, system level and even for field level support, providing that important architectural decisions are made during the system architecture design phase.

The emergence of a variety of system level interface devices from a number of silicon vendors has provided designers with the flexibility to extend to system level the boundary-scan test capability already implemented within their design architecture, in support of a manufacturing board test strategy.

This system level test architecture can be utilised to provide enhanced diagnostic capability and a more flexible test capability as detailed below.

- Provide single-point access to multiple scan chains in support of a partitioned diagnostic capability, for optimising in-system configuration of: cPLD and FPGA devices and for optimising memory read/write cycles for programming flash memory.
- Support a board-to-board interconnect test strategy which can diagnose backplane interconnect test failures to edge connector pin level.
- Accommodate system checkout prior to shipment to customers including verification of firmware objects and facilitate firmware upgrades within a field environment.
- Provide an infrastructure to exercise the embedded test structures that have been implemented within FPGA’s and ASIC’s in support of a SOC device level architecture.
- Provide a single point access capability in support of environmental stress testing and accurate pin level diagnosis.

Topologies and Supporting Devices

The selection of a boundary-scan system level architecture for routing the test access port (TAP) signals is extremely important as it will dictate which system level access devices are selected and the respective implementation requirements. There are 3 major TAP routing strategies that can be adopted, ‘RING’, ‘STAR’ and ‘MULTI-DROP’.

Multi-Drop Architecture
The most popular system level routing strategy adopted by the industry is MULTI-DROP. In this scheme, the five primary IEEE Std. 1149.1 test access signals TCK, TMS, TDI, TDO and TRST are connected in parallel to all backplane slots within the system configuration.

Each of the slots within this multi-drop configuration will have a unique slot address consisting of six/seven address lines providing up to 64/128 unique addresses, which will be hard-wired within the backplane architecture Figure 1.

Each of the boards within the system configuration is accessed by broadcasting its unique backplane slot address via the primary TDI signal line. The board located in the slot corresponding to the broadcast address will wake-up and allow access to selected local scan chains (LSC’s) via the system device access protocol.

**Supporting Devices**

Demand for a boundary-scan system level test capability has resulted in the development of a variety of supporting devices as depicted by the table, Figure 2 below.

<table>
<thead>
<tr>
<th>Device</th>
<th>Name</th>
<th>Silicon/IP Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTS03</td>
<td>Gateway</td>
<td>Firecron Ltd *</td>
</tr>
<tr>
<td>JTS06</td>
<td>Gateway</td>
<td>Firecron Ltd *</td>
</tr>
<tr>
<td>STA111</td>
<td>ScanBridge</td>
<td>National Semiconductor</td>
</tr>
<tr>
<td>STA112</td>
<td>ScanBridge</td>
<td>National * Semiconductor</td>
</tr>
<tr>
<td>LSC BSCAN-1</td>
<td>Multiple Scan Port</td>
<td>Lattice Semiconductor</td>
</tr>
<tr>
<td>LSC BSCAN-2</td>
<td>Scan Path Linker</td>
<td>Lattice Semiconductor</td>
</tr>
<tr>
<td>Device</td>
<td>Name</td>
<td>Silicon/IP Provider</td>
</tr>
<tr>
<td>--------------</td>
<td>-----------------------</td>
<td>---------------------</td>
</tr>
<tr>
<td>SN54/74LVT8996</td>
<td>Addressable Scan Port</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>SN54/74LVT8997</td>
<td>Scan Path Linker</td>
<td>Texas Instruments</td>
</tr>
</tbody>
</table>

**Figure 2:** System Level Access Device Providers

The ranges of devices identified in the above table are available in a variety of package styles and sizes and operating voltages depending upon the architectural requirements of the customer’s designs. The asterisk* in the table (Figure. 2) denotes vendors that also provide the device function as intellectual property (IP) which can be embedded within cPLD, FPGA or ASIC devices.

Lattice Semiconductor also provides the LSC BSCAN-1 and LSC BSCAN-2 as IP, provided that the target device is a Lattice Semiconductor part in which case the core function will be hard-coded into that device and sold as a pre-programmed part.

**Figure 3.** Local scan chain access.

The primary function of all the devices defined in the table is to provide access from a primary boundary-scan bus to specific local scan chains (LSC’s) selected via the system level device protocol as depicted in **Figure 3**.

The LSC’s can either be selected individually or daisy chained together in any LSC combination i.e. LSC1 and LSC2 or LSC1, LSC2 and LSC3, in order to provide complete flexibility for test partitioning.

This is a particularly useful feature when partitioning board designs in support of the in-system programming of flash memory devices. Under these circumstances the number and length of vectors shifted around the boundary-scan chain on the board should be kept to an absolute minimum in order to optimize the flash programming cycle time.

In this situation the boundary-scan device(s) that have direct access to the flash address, data and control signal nets can be located within a single LSC, and this LSC will only be selected during the flash programming phase, whereas all the LSC’s could be selected for board level interconnect testing.

This test partitioning feature can also be utilised when conducting board-to-board interconnect testing within a backplane environment. In this test scenario it is highly likely that only a few devices will provide the I/O access to the board edge connector.
Subsequently it is only necessary to shift test vectors to the devices responsible for providing the stimulus and capturing the respective responses. In this instance the devices that access the board-to-board interconnect signal nets, can be located in a separate scan chain.

**Architectural Decisions**

It is important that the correct system level interface device is selected that supports the appropriate system test access and configuration requirements, and these issues must be considered during the design phase. These key features can be categorized as:-

- How many local scan ports are required?
- Can the device be accessed within a multi-drop configuration?
- Is there a requirement to perform board-to-board interconnect testing?
- Is there provision to pass-through proprietary boundary-scan test controller signals?
- Can access to multi-vendor in-system configurable devices be achieved using the vendor specific proprietary tool suite?
- Can boards located within a multidrop configuration be uniquely identified?

**How Many Local Scan Ports?**

Depending on the board level architecture it will be necessary to consider how many LSC’s can be accessed by the system level interface device. The minimum is three; however, there are variants from Firecron and National Semiconductor that support in excess of six LSC’s.

**Does the System Level Interface Device Support Multidrop Access?**

If the system level backplane architecture has been designed for multi-drop access, it is imperative that the selected system level access device supports a multi-drop addressing scheme.

**Is There a Requirement to Perform Board-to-Board Interconnect Testing?**

In order to support board-to-board interconnect testing it will be necessary to PARK all selected unparked local scan ports (LSP’s). System level interface devices that support the PARKPAUSE instruction will place all unparked LSP’s in one of the TAP controllers pause states; either PAUSE-IR or PAUSE-DR.

Once the appropriate test patterns have been shifted into the boundary-scan registers of the respective backplane interconnect test interface devices, the target devices can be placed temporarily in the PAUSE-DR TAP state.

Subsequently multiple boards within a backplane configuration can then be sequenced through the Update and Capture states simultaneously, thus allowing interconnect tests to be conducted between boards located within multiple slots.

**Is There Provision to Access Proprietary Test Controller Signals?**

Dependant upon specific board designs; it may be a requirement to be able to gain access to proprietary test signals from the boundary-scan test controller provided by your tools vendor.

These signals would normally be directly accessible via the board edge connector to specific local
scan chains; however, by placing a system interface device between the primary boundary-scan bus and the local scan chains, these signals may no longer be accessible.

An example of this test scenario is the use of JTAG Technologies proprietary AutoWriteTM signal to optimize the programming of flash memory.

![Figure 5. AutoWrite pass through. Click here to view a larger image.](image)

During flash memory write cycles the AutoWriteTM signal replaces the WE signal from the flash memory controlling device with a WE strobe. To utilise this feature the system level interface device must be able to route this signal through to the appropriate local scan chain as shown in Figure 5.

**Does the System Device have a Generic Pass-through Capability?**

It may be necessary to access cPLD or FPGA devices located in local scan chains, directly using vendor specific JTAG programming or emulation tools.

However, it is unlikely that this will be possible if a system level interface device is located between the primary JTAG port and the LSC’s, because the vendor specific programming/emulation tools do not support the protocols necessary for communicating with the system interface devices.

Under these circumstances a generic pass-through capability is required which can either be selected by the appropriate binary combination on specific control lines in conjunction with a pass through enable signal, or in the case of the National Semiconductor STA111, by shifting the TRANSPARENTn instruction into the bridge device instruction register (where n is the selected LSP).

As the bridge device state machine moves into the Run-Test-Idle (RTI) state, all the LSP signals selected by the TRANSPARENTn instruction will follow the primary backplane signals, such that the bridge becomes transparent.

**How do I Read the Board ID and Version?**

Depending upon the adopted system level architecture it may be necessary that after establishing a board is present in a unique backplane slot location, to have the capability to read back the identity and version of the board residing in that slot.

This is particularly important within a system architecture where any board type can be located within any of the slots, which means that the board type and version must be established before the appropriate test vectors can be broadcast to that slot address.
**Additional Features**

A number of the system level interface devices have additional features, such as LSP_ACTIVE or BRIDGE_SELECT signal pins which are asserted once the device is selected. This feature can be utilised to control devices that are not fully 1149.1 compliant i.e. devices that do not provide dedicated 1149.1 signal pins, but multiplex these signals with mission mode signals.

In these circumstances specific boundary-scan enable pins must be accessed in order to force the device into the boundary-scan mode of operation or glue logic must be controlled, so that boundary-scan tests can be executed successfully.

The LSP_ACTIVE and BRIDGE_SELECT control signals can be used specifically for this purpose.

**Embedded Vector Delivery**

All the discussions so far have focused on implementing a board level architecture that will support a system level test strategy which utilises an external controller to provide the vector delivery to boards residing in backplane slots addressed by a broadcast address.

The following discussion will address the different backplane architectures that are commonly implemented to support an embedded vector delivery test strategy. These are as follows:-

- Passive Backplane – Local Test Bus Master
- Passive Backplane – System Test Bus Master
- Active Backplane
- Passive Backplane – BIST Sequencer

**Passive Backplane – Local Test Bus Master**

![Figure 8. Passive backplane—local test bus master.](image-url)

In this configuration each plug-in module/board(s) has its own Test Bus Master (TBM) as shown in **Figure 8**, which has full access via the System Level Interface device to all the local scan chains.

The boundary-scan test vectors will be stored locally in flash memory and will be accessed via the TBM under control of the on-board processor.

Hence, each plug-in module is independently and concurrently performing a self test. Inter-board interconnect testing is possible but all TBM’s must be synchronized or one board within the backplane configuration must become the Master.
**Passive Backplane – System Test Bus Master**

In this configuration one module in the backplane is the system Master and all the other modules become Slaves to the system Master as shown in Figure 9.

![Figure 9. Passive backplane—system TBM. Click here to view a larger image.](image)

The boundary-scan tests vectors for testing the slave modules individually or for performing board-to-board interconnect tests are broadcast serially across the primary JTAG bus under the control of the system Test Bus Master.

**Active Backplane**

In the configuration shown in Figure 10, the backplane becomes active with the Test Bus Master, microprocessor and flash memory containing the embedded test vectors located on the backplane.

![Figure 10. Active backplane. Click here to view a larger image.](image)

This allows the TBM master controller to be isolated from all the plug-in modules, allowing a full multi-drop architecture to be implemented.

**Passive Backplane – BIST Sequencer**

The limitation with the System TBM and Active Backplane architectures is that test vectors must be shifted serially from the TBM across the primary JTAG bus to the relevant slave modules within the backplane configuration.

This could result in an excessive amount of data, particularly if the test vectors are performing full...
module interconnect tests or the in-system configuration of cPLD’s or FPGA devices.

If the relevant test vectors were stored and executed locally as described for the Local TBM configuration, the amount of data broadcast across the primary JTAG bus is minimized.

The ability to execute locally stored test vectors sequentially without the overhead of the on-board processor, will free-up the processor to perform other operations.

Firecron Ltd based in the UK, in conjunction with Motorola NSS developed a BIST Sequencer, a non-intelligent device which sequences the shifting of test vectors to and from the local scan chains as selected by the local system interface device as shown in Figure 11.

![Figure 11. Passive backplane—BIST sequencer.](Click here to view a larger image.)

This solution which is ideally suited for localized embedded test vector delivery and in particular for accessing the embedded test structures within SOC architectures has been implemented within Motorola’s 3G Base Station products.

These embedded test cores can be accessed through the SOC device 1149.1 TAP port and exercised using a simple RUNBIST instruction. Once the BIST routine has completed, the resultant test signature is compared against the expected default signature and the appropriate PASS/FAIL status reported through the BIST status register.

More detailed analysis of failures, as well as the selection of enhanced diagnostic algorithms is available through alternative test instructions, and these could be exercised once the faulty line replaceable unit (LRU) has been returned to the service depot for repair.