With the proliferation of wireless products, chip designers are increasingly required to integrate RF and digital functions within single system-on-chip (SOC) implementations. This integration melds disparate functional blocks that traditionally have been tested on dedicated RFIC and digital-logic test systems. In addition, it requires close cooperation between two engineering groups—digital and RF engineers—who have traditionally worked alone.

Of course, many digital engineers aren’t unfamiliar with high-frequency signals, as digital clock rates extend beyond 1 GHz. According to Karl Watanabe, senior SOC product engineer at Advantest, today’s high-speed digital designs are employing techniques that RF designs have incorporated for two decades. Nevertheless, the measurement techniques applicable to gigahertz-clock-rate digital designs differ significantly from those of gigahertz-rate-carrier-frequency RF designs.

**RF implies slow clocks—for now**

If there’s good news, it’s that you won’t have to contend with microwave and high-frequency components within a single device, at least not today. According to Alan Kafton, strategic consultant at Agilent Technologies, designers of devices for mobile-communications applications invariably must contend with power management and, consequently, try to confine digital clock frequencies to the megahertz ranges.

The low-frequency-digital safety net may soon disappear, however, as third-generation (3G) wireless technologies take hold. (See the Glossary on p. 19 for explanations of the abbreviations used in this article.) Emerging 3G devices require lots of processing power, demanding ever-higher clock frequencies, even at the expense of power consumption. As these frequencies increase, says Ken Lanier, director of marketing at LTX, concomitant signal-integrity issues will arise. Even with 60 dB of isolation, he says, a high-speed 3-V digital signal isn’t sufficiently attenuated to prevent it from mimicking a significant interfering RF signal. Providing more isolation to minimize crosstalk will require additional load-board layers and the use of differential RF and digital signal paths, Lanier notes.
Semiconductor ATE vendors are offering a variety of SOC test platforms that can address digital and RF test chores (Table 1). But you can't count on buying a turnkey, plug-and-play test system that's ready to test the Bluetooth, wireless-LAN, and other digital-baseband-plus-RF radio chips hitting your production floor. In fact, if digital/RF SOC designs have been released to production without the participation of test engineers, it may already be too late to effectively use the "one-platform-fits-all" ATE system that you hoped would solve all your test problems for years to come. If you are encountering mixed digital/RF configurations for the first time, you would do well to familiarize yourself with various aspects of the product life cycle, from design through test-platform selection, test-program development, wafer-level test, device-interface-board design, and package test.

Stuck at 2.40712 GHz?

Developing an effective test involves much more than swapping out pin cards to provide the instrumentation your device under test (DUT) requires. It begins with chip design itself. Design for test (DFT) and built-in self-test (BIST) can significantly ease digital tests (Ref. 1), and you should ensure that those techniques are embedded in the digital portions of your devices. But BIST tools are nearly nonexistent for RF functions, which also lack well-defined DFT approaches analogous to, for example, logic test's scan insertion. Agilent's Kafton notes that RF designs simply aren't amenable to the types of DFT that can benefit logic designs. Take fault models: Although a few fault-model abstractions (for example, "stuck-at-one" and "stuck-at-zero") do a good job of representing the physical defects likely to appear in logic devices (Ref. 2), RF components would require an infinite number of fault models, Kafton points out.

Nevertheless, don't abandon RF DFT approaches completely. You should urge designers to consider implementing ad hoc RF DFT approaches, such as providing loopback capability and wafer-level access to internal analog and RF nodes. Kafton explains that a single-chip Bluetooth device (Ref. 3) would have a low-noise amplifier whose output wouldn't normally be available as an output of the packaged device, but designers could make this node available for wafer-level test probing. David Derian, wireless/RF marketing manager at Teradyne, says some of his customers have innovative approaches to enabling test of phase-locked loops: They have built in the necessary structures to test permutations of digital dividers and to determine whether the devices achieve proper RF frequencies within allowed settling times and with acceptable levels of phase noise.

In addition to different levels of DFT friendliness, there are other natural barriers between RF and digital test. At the most basic, says Gordon Dewitte, '93000 SOC Series product manager at Agilent Technologies, "RF tests typically take place in the frequency domain, while digital tests typically take place in the time domain." According to Advantest's Watanabe, if you have an RF test background, you'll "need to learn about scan test, ATPG, and embedded-memory test." An RF partisan, Watanabe suggests that digital engineers will have a harder time adapting to the combined RF and logic test environment: "Unlike the quick information, such as setup and hold times, you get from digital devices, RF measurements require mathematical analysis to yield meaningful results. Digital test engineers will have to immerse themselves in the world of DSP and mixed-signal test. Deriving test data from Bluetooth, CDMA, GPRS, GSM, and W-CDMA devices is a math-intensive process requiring complex waveform creation and response-signal digitization."

But RF test engineers also may have to adapt to test modern wireless devices. John Lukez, wireless product marketing manager at Credence Systems, says that tests involving pure sine-wave stimulus signals are no longer adequate for characterizing wide-bandwidth digitally modulated carriers (Ref. 4). Consequently, you'll want to evaluate whether your test instrumentation can adequately mimic and analyze real-world wireless-transmission signals.
Combined RF and logic tests required

With digital and RF test engineers having their hands full within their own domains, you might be tempted to try to separate digital and RF functions, testing each separately. You might want to turn off the RF and test the digital circuitry and then suppress the digital clock and test the RF elements. Unfortunately, you'll find that RF and logic tests on an SOC can't be compartmentalized in that manner, as one designer, Paul van Zeijl of Ericsson Eurolab Netherlands (Emmen, the Netherlands), told attendees at the 2001 Design Automation Conference (Ref. 5).

Figure 1. Keeping the load board simple is a key to successful digital/RF test. One way to do that is to employ a test system that accommodates mixers and other RF components. Courtesy of Agilent Technologies.

Figure 2. Shielding within the device-interface board helps to preserve signal integrity in combined RF and digital tests. Courtesy of Teradyne.

Ultimately, says Derian at Teradyne, the questions a radio-transceiver test system must answer include these: "Is the device able to transmit a signal clearly without polluting the spectrum with unintended products, and is the device able to receive the intended signal in the midst of a lot of..."
clutter from other transmissions and environmental noise?" To answer the first of these questions, you need a test system that can test modulation quality and adjacent-channel power ratio (ACPR); to answer the second, you need a test system that can generate a modulated test signal as well as jammer or adjacent signals.

But the transmission and reception don't take place in a pure microwave world. Indeed, they take place in close coordination with—and in fact under the control of—digital commands. If you suppress the digital commands, you'll stifle the RF activity you're trying to measure. As a first approach to accommodating the two domains harmoniously within your test system, Agilent's Kafton recommends keeping the device interface board (DIB) as simple as possible (Figure 1): Put multiplexers, combiners, splitters, and other components within the test system. That ensures that errors associated with these components can be corrected for by tester calibration. In addition, it frees up DIB real estate for multisite testing. (Ref. 6 provides more information on DIB design.)

Derian notes that all-RF or all-digital DIBs have traditionally been two-dimensional in their signal-delivery method—signals have traveled on 2-D traces on the DIB surface or within its multiple layers. That approach is breaking down with mixed digital and RF signals, however, and he recommends placing DIB RF connectors as close as possible to the DUT. Furthermore, he adds that DUT shielding (Figure 2) can improve signal integrity.

Running the tests

Of course, the DIB is merely a conduit for carrying test signals between tester and DUT. The tester itself must generate test signals to apply to the DUT and detect and analyze its responses. To that end, it must embody the digital and RF instrumentation necessary to represent the real-world environment in which the DUT will ultimately work. To make your test chores easiest, you'll want to choose a system that provides close coordination of digital and RF events.
A Bluetooth chip, for example, provides RF-output frequency hopping (Figure 3) under the control of Bluetooth digital protocol commands. You could use rack-and-stack instrumentation for Bluetooth testing, using digital pattern generators to apply the frequency-hopping commands while using RF instruments to monitor the response, but the delays inherent in rack-instrument control schemes (such as IEEE 488 control) can inject delays that make it impossible to adequately correlate digital and RF events. Michael G. Lohrer, VP of operations at Programmed Test Sources (Littleton, MA; www.programmedtest.com), offers signal sources with optional IEEE 488 interfaces that customers could use to implement their own test systems, yet Lohrer says the most typical scenario is for ATE companies to buy his instruments and integrate them into a complete ATE system for the end customer.

A complete system (such as that shown in Figure 4) can integrate all the necessary instrumentation under the control of a single software tool that can help you develop and perform tests quickly and accurately. Make sure you choose a system that provides the necessary digital and RF pin counts. Table 1 indicates the range of capabilities available.

Table 1. Representative RF plus digital test systems

<table>
<thead>
<tr>
<th>Company</th>
<th>Tester</th>
<th>Digital pins</th>
<th>Analog pins</th>
<th>RF ports</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advantest, Santa Clara, CA 408-988-7700; <a href="http://www.advantest.com">www.advantest.com</a></td>
<td>T7610</td>
<td>32 max at 20 MHz max</td>
<td>—</td>
<td>4 max at 8 GHz max</td>
</tr>
<tr>
<td>Agilent Technologies, Santa Clara, CA 800-452-4844; <a href="http://www.agilent.com">www.agilent.com</a></td>
<td>93000</td>
<td>1024 max at 1.6 GHz max</td>
<td>64 max</td>
<td>12 max at 8 GHz max</td>
</tr>
<tr>
<td>Credence Systems, Fremont, CA 510-65-7400; <a href="http://www.credence.com">www.credence.com</a></td>
<td>RFx</td>
<td>32 max</td>
<td>—</td>
<td>8 max at 6 GHz max</td>
</tr>
<tr>
<td>Eagle Test Systems, Mundelein, IL 847-36-8282; <a href="http://www.eagletest.com">www.eagletest.com</a></td>
<td>ETS-600</td>
<td>256 max at 50 MHz max</td>
<td>308 max</td>
<td>32 max at 6 GHz max</td>
</tr>
<tr>
<td>LTX, Westwood, MA 781-461-1000; <a href="http://www.ltx.com">www.ltx.com</a></td>
<td>Fusion HF</td>
<td>1024 max at 500 MHz max</td>
<td>64 max</td>
<td>16 max at 8 GHz max</td>
</tr>
<tr>
<td>SZ Testsysteme, Amerang, Germany +49-8075-170; <a href="http://www.sz-testsysteme.de">www.sz-testsysteme.de</a></td>
<td>Kodiak</td>
<td>384 max at 200 MHz max</td>
<td>64 max</td>
<td>16 max at 6 GHz max</td>
</tr>
<tr>
<td>Teradyne, Boston, MA 617-482-2700; <a href="http://www.teradyne.com">www.teradyne.com</a></td>
<td>Catalyst</td>
<td>1024 max at 1.6 GHz max</td>
<td>20 max</td>
<td>16 max at 6 GHz max</td>
</tr>
<tr>
<td>Third Millennium Test Solutions San Jose, CA 408-435-1788; <a href="http://www.3mts.com">www.3mts.com</a></td>
<td>3M10</td>
<td>200 max at 80 MHz max</td>
<td>200 max</td>
<td>16 max at 7.2 GHz max</td>
</tr>
<tr>
<td></td>
<td>RFOC</td>
<td>200 max at 80 MHz max</td>
<td>200 max</td>
<td>16 max at 7.2 GHz max</td>
</tr>
</tbody>
</table>
References


