ITC: Synopsys addresses yield, memory test, and small delay defects

Test Measurement World Staff - October 27, 2006

Synopsys announced links between its TetraMAX ATPG tool and Odyssey yield-management system, touted a collaborative effort with Virage Logic, and said it's working with several customers on small-delay-defect test. In addition, Chris Allsup, marketing manager for test automation products, discussed Synopsys ITC demonstrations in an interview with chief editor Rick Nelson. (Click to hear the interview.)

The links between its TetraMAX automatic test pattern generation (ATPG) diagnostics and its Odyssey yield management system (YMS) are aimed at accelerating yield ramp at foundries. These links will enable high-throughput export of test-failure diagnostics generated by the TetraMAX tool into the Odyssey YMS. Foundries can use the capability to analyze the vast amounts of diagnostics data generated from volume production runs (a capability often referred to as "volume diagnostics") to steadily improve process yield.

"Synopsys considers high-throughput linkage between failure diagnosis data and yield management systems a critical step toward the realization of full-volume diagnostics for production runs," noted Dr. J. Tracy Weed, director of the Manufacturing Enabling Products Group at Synopsys. "The link between TetraMAX diagnostics and Odyssey YMS will benefit both foundries and fabless companies by accelerating yield ramp of their high-volume production ICs."

The TetraMAX diagnostics identify logic in a design that could contribute to observed mismatches in an ATPG pattern set. The Odyssey YMS cross-correlates data sets, exploiting data-mining capabilities to identify underlying physical mechanisms for yield loss. However, collecting diagnostics information for all failing devices in a high-volume production run and building a database to analyze and correlate the failure data has traditionally been a manually-intensive and time-consuming process. The TetraMAX-Odyssey link is designed to streamline yield management of production ICs by facilitating real-time collection and analysis of high-volume failure data extracted from multiple die and wafer lots.
"For years, the TetraMAX solution has provided designers the ability to quickly and accurately diagnose parts with scan-test failures," said Graham Etchells, director of test marketing, Synopsys Implementation Group. "Now we are seeing the TetraMAX solution deployed at leading foundries worldwide as an essential ingredient of their yield learning platforms for nanometer processes. The TetraMAX-Odyssey link is a key enabling technology that will increase the effectiveness of volume diagnostics and streamline the use model."

**Teaming Virage Logic on STAR**

The collaborative effort with Virage Logic (www.viragelogic.com) has yielded a test reference design flow for cost-effective testing and repair of embedded memories for system-on-chip (SOC) designs. The validated test design flow for 90-nm and 65-nm processes is based on the Synopsys Galaxy test platform and Virage Logic's Self-Test and Repair (STAR) Memory System. The reference design flow provides designers an automated solution to address time-to-market pressures and challenges of creating high-quality manufacturing tests for complex designs that contain multiple embedded memories. The collaboration will continue with a second validated Galaxy test reference flow, which will integrate the testing of Synopsys DesignWare IP memories within Virage Logic's STAR Memory System.

"This latest collaboration with Synopsys further validates Virage Logic's commitment to providing customers with integrated design flows that help accelerate their silicon success, particularly as they move to the more advanced process nodes of 90 nm and 65 nm," said Jim Ensell, senior VP of marketing and business development at Virage Logic. "With STAR Memory System customers achieving yield improvements of up to 250 percent, we're confident the new Synopsys-Virage Logic reference design flow will enable our mutual customers to meet their SoC test, yield, and time-to-market goals."

"Today's consumer products often contain dozens if not hundreds of memories and register files," said Bijan Kiani, VP of marketing, Synopsys Implementation Group. "Creating high-quality manufacturing tests that deliver good coverage for the design logic as well as the memory content is a challenging and time-consuming task. The Synopsys-Virage Logic collaboration will help designers address these challenges by ensuring interoperability between Virage Logic's STAR Memory System RTL flows and the test-synthesis flows within Synopsys' Galaxy test platform. Synopsys customers using DFT MAX physical-aware scan compression to reduce test costs and increase test quality will now benefit from a verified, automated flow that includes comprehensive testing of embedded memories."

**Collaboration on small delay defects**

Synopsys also announced that it has collaborated with several semiconductor firms to test a new ATPG technology designed to increase the quality of manufacturing tests by targeting small delay defects. The enhanced capability uses precise timing information from the Synopsys PrimeTime sign-off static timing-analysis tool to test for small circuit delays that could result in timing failures when parts are run at-speed. Because traditional transition-delay ATPG does not directly target small delay defects, the new approach can further improve quality and reduce test escapes for digital integrated circuits (ICs) sensitive to small delay defects.

The Semiconductor Technology Academic Research Center (STARC, www.starc.jp), a research and development consortium founded by major Japanese semiconductor companies, has been working with Synopsys for the past two years to help develop and validate the technology. "STARC considers small delay defects a critical quality issue for our member companies as they design more circuits at 90-nanometer technologies," said Takashi Aikyo, senior manager of the Test and Diagnosis Group at
STARC. "We appreciate the early interest from Synopsys, and we now look forward to working with our member companies and Synopsys to deploy this new test technology on production designs."

"Subtle process variations at 90 nm and below can introduce small delays that adversely affect the most timing-sensitive paths in a design," said Graham Etchells, director of test marketing, Synopsys Implementation Group. "These small-delay defects can remain untested using traditional transition-delay ATPG because it lacks the precise timing information required to explicitly target them. The new technology uses precise timing data from PrimeTime sign-off analysis to test small delay defects. We expect this innovation will result in a significant improvement in the quality of at-speed testing, leading to fewer test escapes and lower test cost."

Highly-accurate timing analysis is the key to testing small delay defects. Designers can pass parasitic information from Synopsys' Star-RCXT sign-off extraction tool to the PrimeTime tool for static timing analysis, then use pin-slack information generated from the timing analysis to create small-delay-defect ATPG patterns. Reports and histograms provide metrics for measuring the test quality of a design in the presence of small delay defects. The new ATPG technology is consistent with existing design-for-test (DFT) methodologies and does not require changes to a design.

www.synopsys.com