Semiconductor process engineers have always understood the need to inspect silicon wafers to identify defects and eliminate them at their source. To simplify the process, semiconductor equipment manufacturers routinely place inspection systems on production lines. These systems can simply show that defects exist at specific locations, or they can capture defect images and measure their characteristics. Inspection-system vendors now face challenges as engineers apply new production technologies and design rules for smaller devices.

"When using 130-nm design rules, engineers didn't consider a 65-nm defect 'big,' nor was it detrimental to process yield," says Wayne McMillan, product marketing manager at KLA-Tencor's Surfscan division. "But when 65-nm design rules apply, a 65-nm defect will definitely affect yield. "Inspection resolution must keep up with the ever-smaller defects semiconductor manufacturers need to find. Manufacturers must eliminate these new and smaller defects in their processes and in their fab tools as early as possible to keep yields high. (In the semiconductor industry, the term "fab tool" describes a self-contained module that incorporates actuators, vacuum systems, wafer handlers, chemicals, and electrical power. A fab tool takes part in the automated semiconductor-fabrication process.)"
You might think because semiconductor-device geometries continue to shrink, optical inspection could not keep up. After all, wavelengths determine resolution limits. But Leica Microsystems recently introduced a 248-nm wavelength deep-UV inspection system that offers 80-nm resolution (Figure 1). According to Volker Knorz, Leica's director of product management and support, the next step involves moving to a 193-nm wavelength that lets an inspection system resolve defects of about 60 nm.

Often, the demands for greater resolution go hand in hand with those for higher inspection speeds. A 300-mm wafer carries more than twice the area of a 200-mm wafer. So, to keep wafers moving at a reasonable rate through a 300-mm fab, inspection equipment must operate faster. But as transistor sizes get smaller, process engineers also demand that inspection systems locate and identify smaller defects, which requires additional time. Many inspection systems let engineers make a time vs. resolution tradeoff. Nanometrics, for example, quotes a rate of about 150 wafers/hr when inspecting for 0.5-µm (500-nm) defects, but the rate drops to 50 wafers/hr for 50-nm defect inspections. Inspecting 300-mm wafers and some 200-mm wafers also requires a thorough inspection of the wafer's back side (Figure 2). Keep in mind that although an inspection system will inspect an entire wafer, semiconductor vendors do not usually inspect every wafer.
"Process engineers must distinguish between defect detection and defect imaging," notes Dr. Barry Bowman, a member of the technical staff at Nanometrics. "Imaging means you take a picture with sufficient optical resolution to measure what you see. But to detect a defect, you don't need high optical resolution because you only look for the intensity of scattered light." Even equipment that only detects defects requires calibration, and standard-size detection systems and standard-size polystyrene latex (PSL) spheres deposited on test wafers provide the means. "If your equipment can detect a certain size PSL, it can detect a defect of comparable size," says Bowman. A Nanometrics system, for example, can detect PSL spheres down to 50 nm on bare wafers.

In addition to detecting and imaging defects, inspection systems will map them so process engineers can relate defect types to specific process steps or fab tools. The defect information can form part of a statistical process control (SPC) loop that keeps process variables within specifications. Inspecting for defects also may help ensure quality control as wafers move outside a fab.

"People have talked about linking the front end [input] and back end [output] of the semiconductor-manufacturing process, but not many people do it," says Ardy Johnson, VP of marketing at August Technology. "A back-end contractor wants to measure the quality of incoming products so it's not held accountable for defects present on wafers it receives. Likewise, the client wants to ensure it receives wafers back from the contractor without any defects caused by the contractor." The images in Figure 3 show typical defects on semiconductor devices.

The demands for better resolution and faster imaging speeds accompany almost every decrease in semiconductor geometry. Now, the demands of new technologies such as silicon-on-insulator and strained silicon, as well as the need to inspect wafer edges, present challenges for inspection-equipment vendors.

**Nicked and scratched**

A minor defect on a wafer edge, perhaps a scratch or nick invisible to the naked eye, can cause a wafer to shatter in a processing oven. The thermal stress starts a crack or cracks that propagate through the silicon wafer. It costs manufacturers a great deal to shut down a fab tool, clean out broken wafer bits and contaminants, and get the tool running again. Semiconductor fabs see wafer-edge inspection as a way to identify, and, if necessary, weed out defective wafers.
Figure 3. These images show typical defects found on processed wafers, such as a-top) bridged metal, b-middle) residual metal, and c-bottom) a scratch across an IC. Courtesy of August Technology.

Semiconductor manufacturers usually receive defect-free wafers from suppliers, so most edge-related problems stem from damage in a fab tool. Robotic wafer-handling equipment can inadvertently damage a wafer simply by gripping it, incomplete processing can leave residues on
wafer edges, and so on. Thus, when process engineers detect an edge defect, or a series of similar defects, they employ additional inspection systems to trace the problem to a specific fab tool that may require maintenance.

Larry Schott, a product manager at Hologenix, says process engineers want to detect and automatically classify edge defects such as pits, scratches, cracks, photoresist and chemical-mechanical polishing (CMP) residue, and so on. These classifications can help identify what caused the defects. Schott explains, "Process engineers set up criteria to accept or reject wafers based on quantities and sizes of specific types of defects."

But edge inspection gets complicated because wafers come with different edge profiles. Wafer manufacturers produce wafers with various bevel angles, and some wafers come with rounded edges. An inspection system must completely inspect all edge surfaces. "We use as many as 10 cameras in our system for edge inspection," says Hologenix's Schott. "We employ five cameras to inspect just the wafer-orientation notch, a 1x2 mm fiducial mark on 300-mm and 200-mm wafers."

Also, semiconductor and wafer manufacturers often want equipment to inspect within the exclusion zone—a 1-mm band, or ring, along the outside edge. Handlers or operators can touch a wafer only in this small area. Many laser-based inspection systems can't inspect that close to an edge, though. Reflections from the edge reduce the effectiveness of laser measurements and adversely affect defect detection.

**Expand a lattice**

New semiconductor processes also challenge inspection-system suppliers. IC manufacturers always seek new technologies that will increase the performance of semiconductor devices. In some cases, a die shrink does the trick, but often manufacturers must look for something new. Two new processes, strained silicon and silicon-on-insulator (SOI), can increase transistor switching speeds and decrease power consumption.

Manufacturers now produce sample quantities of strained-silicon and SOI ICs using 90-nm design rules, and IC vendors expect to see widespread application of both technologies in designs that use 65-nm design rules.

Strained silicon relies on a substrate of silicon doped with germanium. The process starts with an epitaxial layer of silicon about 2 µm thick. Further deposition increases the germanium concentration. After doping the silicon, depositing pure silicon on the silicon-germanium substrate produces a silicon crystal lattice in which the silicon atoms have a 1% greater atom-to-atom spacing. That small change increases electron mobility and transistor switching speed. Intel, for example, uses this type of strained silicon to obtain a 20% performance increase in some microprocessor ICs.

During production of the silicon-germanium mix, the added germanium causes crystal dislocations and the atoms arrange themselves to relieve strain. These dislocations can "pile up" in one place and greatly reduce yield. Unfortunately, they're difficult to detect using current inspection techniques.

In addition, strained silicon exhibits the same defects that occur on standard epitaxial silicon—crystal defects, shallow stacking faults, particles, and so on. "Crystal defects and stacking faults are yield killers," says KLA-Tencor's McMillan. "It's critical that process engineers find these defects so they can improve their process." KLA-Tencor's SP1 uses laser scattering to inspect strained-silicon wafers. The instrument detects defects and stacking faults and distinguishes them from other types of defects.
Lay on the oxide

The need for low-power and high-speed devices—think of video cell phones—has fueled the interest in SOI, a technique that produces silicon semiconductors on an insulating layer of silicon dioxide. But SOI can cause inspection headaches.

IBM, AMD, and Motorola already use an SOI process to produce ICs, and other IC manufacturers will adopt similar processes to increase transistor speeds as designers move to 65-nm design rules. The SOI isolates the transistors from the bulk silicon, which reduces parasitic capacitance and lets transistors operate at higher frequencies. The transistors also use less power than those built on bulk silicon.

Wafer suppliers produce SOI wafers using one of two processes: a bonding approach that sandwiches silicon and silicon oxide layers and then cleaves away an SOI wafer, or a process that implants oxygen into a bulk-silicon wafer to produce an insulating layer. The latter goes by the name "separation by implantation of oxygen," or SIMOX.

Producing SOI wafers also introduces standard defects, such as stacking faults, particles, and holes. But the thin SOI layers also cause a problem inspection companies have yet to overcome: They produce optical interference patterns that decrease imaging resolution. The differences in the refractive indices of the silicon and the buried oxide (BOX) layer create the patterns, whose characteristics depend on each layer's thickness, which can vary slightly across a wafer's surface. IC manufacturers also vary thicknesses to meet semiconductor performance specifications.

So, depending on the thickness ratios, engineers get different imaging resolutions, which affect an inspection system's ability to accurately measure defects. Although customers seek consistent high-resolution measurements, no way currently exists for overcoming the 'layer sensitivity' when inspecting SOI wafers, although companies are working on the problem.

Given the individual challenges of SOI and strained silicon, imagine what will happen as engineers combine these techniques and apply 45-nm design rules to new designs. Yet again, they'll challenge inspection-system vendors to develop novel inspection equipment.

Manufacturers of wafer-inspection systems

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