Circuit measures on-chip jitter

Martin Rowe - May 01, 2004

Every component that generates and transports serial data streams contributes jitter, but you can minimize jitter in components if you can measure it. Using circuit simulation, researchers at the University of Vermont have developed a circuit that measures average jitter in an IC. In a paper published in the December 2003 issue of *IEEE Transactions on Instrumentation and Measurement*, Xia and Lo developed a simulated jitter-measurement circuit (see upper box in figure) for measuring jitter in phase-locked loop circuits (lower box). IC designers can incorporate this circuit into new designs.

A charge pump, capacitor ($C_p$), and comparator set a logic state, which causes a counter to increment or decrement based on jitter levels. *Courtesy of IEEE.*

The circuit measures average jitter by converting timing variations between signal edges into an analog voltage. It then compares that voltage to a reference voltage, from which it increments or decrements a 4-bit counter.

The measurement circuit's charge pump consists of a current source ($I_c$) and a current sink ($I_d$). Switches S1 through S4 cause $C_p$ to charge or discharge. When S1 and S2 close while S3 and S4 open, $C_p$ charges, indicating an increase in jitter. If jitter decreases, S1 and S2 open and S3 and S4 close, and $C_p$ discharges. A comparator compares the voltage of $C_p$ ($V_{inn}$) to a reference voltage ($V_{cent}$). A reference clock ($S_{ref}$) controls S1 and provides a clock for the D flip-flop. Thus, the flip-flop's output updates once per $S_{ref}$ cycle. When jitter levels change polarity, the $V_{ncmp}$ causes the 4-bit counter's value to increment or decrement, providing a digital representation of the average jitter.

Reference