ALLENTOWN, PA—Developing an effective design and test strategy for an IC can be a daunting task. At Agere Systems, the difficulties are magnified because the company produces hundreds of distinct devices, with 200 or so designs having been completed within the past year and a half. Each product benefits from a particular design and test strategy, which involves identifying an appropriate ATE system as well as an optimal combination of design-for-test (DFT) and built-in self-test (BIST) technologies.

Supporting the company's four divisions—Enterprise & Networking, Mobility, Storage, and Telecommunications—Lou Ternullo and John Matthias are part of teams that serve as central resources that can help each division most effectively meet its design and test goals. Ternullo, technical manager for DFT and IP in the company's design-platform organization, is responsible for BIST and DFT tools, while Matthias, distinguished member of the technical staff in the IC test technology group, is responsible for automated test equipment (ATE) and benchtop debug tools.
Ternullo explained, "My team's charter is to stay on top of the DFT tools that are available in the market. At the same time, I work with John's team," which is concerned with the back end of the production and test process, "to ensure that design and test tools play well together." Because no team has the resources to extensively evaluate every DFT and BIST tool on the market, he said, "We try to intelligently determine which DFT tools may add value to our flow through press articles, news releases, and of course, vendor visits."

What's up-and-coming now, he said, are more advanced automatic test-program generation (ATPG) tools, which include at-speed ATPG and compression techniques in addition to BIST tools, such as ones from LogicVision.

John Matthias prepares to debug a BIST-enabled device under test using a LogicVision Validator benchtop tester.

Agere employs a combination of electronic design automation (EDA) tools, and Ternullo cited the benefits of a multivendor approach. "We have contracts with multiple EDA vendors," he said, adding that multiple sets of tools help to provide a good balance to help Agere's design team meet various design challenges. "Vendor A's tools may work better to help meet a customer's specification on one design," he said, "whereas vendor B's tool may prove to be better for a different design. In addition, one vendor's tools may be more up to date with respect to certain features." Having multiple vendors, he added, also helps to increase competition, which in turn fosters regular tool improvements.

He also noted that in addition to having expertise in available commercial tools, Agere, with its AT&T Bell Labs and Lucent heritage, can apply its own technologies. "We had our own DFT development team years ago, with our own ATPG, logic BIST, memory BIST, and boundary-scan tools. Having the knowledge from our DFT tool development days helps my team better assess the value-added features in the tools we use and evaluate. We like to stay on par with our vendors in order to add value for our customers."
A modified board employs banana jacks and other connectors to provide a Validator benchtop system with access to power and ground planes, high-speed clocks, and the test access port.

Using memory as an example, he said, "We work with DFT vendors who typically do not have memory expertise as well as memory-design companies and compiler companies that typically do not have DFT expertise. In working closely with them, we ensure that their solutions, first, fit into our flow and, second, are being used optimally to test our chips. We work with them on adding value to their tool. We do a lot of testing of beta code on new releases of software, and there's a lot of give and take. They won't do everything we request. But the features they agree to develop help add value to Agere designs."

In cases where vendors cannot provide Agere with a cost-effective solution, Agere designers sometimes rely on internal expertise. For example, Ternullo said, "One customer required the use of a ternary CAM [content addressable memory] in its design, and no commercial tool vendors offered a competitive BIST solution. That's where our in-house expertise paid off. We internally developed a BIST engine to test ternary CAMs. Developing our own BIST controller is not always the most practical solution, but it's one way Agere can add value to its DFT offering."

**Serving internal customers**

Knowledge of available commercial tools and in-house expertise helps Ternullo's group meet its primary goal, which, he said, "is to support our own customers, which are the internal divisions here at Agere, throughout the DFT flow. Our efforts begin with what we call test architecture review." Within the design community, he said, there's persistent resistance to DFT and BIST unless "it has no impact on area and performance, and we know that's not possible. But we can minimize DFT disruptions by working with chip architects early on to map out functional blocks and determine how to interface them with the test technologies we plan to use. Early involvement will help avoid the need to repartition the design to accommodate DFT further downstream in the design cycle when it becomes more difficult. We continue working with chip designers throughout the DFT insertion process to help improve Agere's chances of success."
The exact status of a design when Ternullo's group gets involved depends on the product line. "Agere has what's referred to as 'standard products' and ASICs. Agere develops standard products internally and typically has access to all the RTL code. On an ASIC product, we typically start with a gate-level netlist. Whatever the case, we like to see at least a high-level block diagram that provides some general idea of the partitioning.

"When we do get to the floor-planning stage, we may modify the logical or physical partition. For example, we will attempt to share memory BIST controllers as much as possible between like memories to reduce area, or we may make tradeoffs in test time by testing some memories serially and others in parallel. These are all tradeoffs we address up front. We can't know for sure that we've made the right choices until we achieve timing closure, but by being involved from the beginning, we can minimize the number of iterations required to complete a DFT-inserted design."

Doug Rabold, test center facilities engineer, sets up a Teradyne UltraFlex, one of approximately 35 ATE systems used for test development at Agere's Allentown test facility.

Of course, multiple-vendor flows do have drawbacks. Said Ternullo, "We would love to have one tool set that would satisfy our DFT needs from end to end in the design process—allowing us to do analysis at the front-end architecture level all the way to the back end, including field returns." EDA vendors' marketing messages might suggest such a tool exists, but Ternullo and Matthias both agree that it doesn't. Said Ternullo, "Part of what my team does is cut through the marketing fluff and see where the rubber meets the road." One tool, he said, might make it very easy to insert DFT, and that tool would make designers happy by getting to tape-out quickly. "But if as a result of using that tool it takes weeks to bring the test program up on an ATE system, then the savings gained on the front-end are wasted." The same is true for the reverse, he added, where the savings of an easy-to-brig-up test program might be more than offset by a difficult, costly, and time-consuming DFT-insertion phase.

So, said Ternullo, his team evaluates the effect of a tool from architecture conception, DFT and BIST insertion, and validation to bringing up first silicon, debugging it, and developing production-test programs. To that end, he works closely with Matthias, who said, "We are tearing down the wall between design and test. Maybe it's not 30 feet high anymore, but it's still there." Said Ternullo, "John and I are in totally separate organizations, with our reporting chains meeting at the executive level. But we do not let that get in the way of doing what is right for Agere. We work together to resolve issues to the benefit of both the front-end and back-end teams. A lot of what we do is internal marketing to the divisions."
Supporting production

For his part, Matthias is part of the global operations team, which supports manufacturing, beginning at the point where a product tapes out and continuing throughout the production life cycle. Agere has adopted a "fab light" strategy, in which it increasingly employs external foundries, but it nevertheless retains about 95% of assembly and test functions in house. Agere does outsource some packaging and test of some high-volume parts, but Matthias said that keeping test in house is cost-effective and makes it easier to serve end customers, who are putting packaged parts or bare die on printed-circuit boards. With the test function in house, he said, Agere can quickly respond if customers experience a problem such as high line fallout or high return rates. "We can get involved quickly to get to the root cause of the problem."

Matthias said global operations includes everything from supply-chain management to shipping. Within that operation, he said, "My particular group, test technology, is a very small group of experienced people who have been in the test world for typically 15 years or more. One of our primary responsibilities is forward-looking—what's the next technology we have to prepare for? What's the next type of product we will manufacture, and what equipment will we need to test it?"

To prepare for future products, he studies the internal roadmapping of Agere's design teams and keeps tabs on what ATE and EDA vendors are doing. "We are very proactive with our ATE vendors, working with them 12 to 18 months ahead so that we can get them on the same roadmap for developing their tools to support what we have coming."

Matthias continued, "Anything we believe will give us an advantage in getting product to market faster and resolving customer problems faster is something that I am interested in. So, I work really closely with Lou, and I get involved early with some of the design teams." He tries to head off problems such as an engineer embarking on a design that might require a 10-Gbps signal from an ATE system. "I say, time out. Let's discuss your specific test needs, what the ATE can provide directly, and what we might need to augment with other components or instrumentation. And we work out test strategies that we can support with our existing production equipment."

Is there a move within Agere to outsource assembly and test, as some companies do (Ref. 1)? According to Matthias, "We've been doing [assembly and test] internally for a long time and have a large installed base of capital equipment. We've evaluated this extensively, and our conclusion has always been the same: there are key advantages to maintaining these functions in house. We do outsource some amount of assembly and test, but we still see significant economical and operational advantages to keeping a major portion of this function in house. The test houses have flexibility in that they have a lot of different equipment and are willing to reconfigure it to test a certain product, but they don't necessarily have the test-development expertise we have, and they certainly don't have the knowledge of the device design. By keeping these functions in house, if a problem arises, we don't have to try to coordinate our troubleshooting efforts across multiple different companies."

Matthias cited as an example a defective-parts-per-million (DPPM) problem in a customer's production line that resulted in elevated levels of field returns. "We've done a lot of ASICs for modems and Ethernet cards that are being sold to consumers by the millions. If you buy a modem or network-interface card from company A and it doesn't work, you send it back to company A. If company A's engineers identify what they think is a DPPM problem with a part that we supplied, then we get involved. I have actually gone to customer production facilities to investigate their production lines and help resolve such issues—not to say, 'it's your problem, not mine,' but to get to the bottom of whatever the problem is. We've found the gamut of issues: Some have been assembly-related, some have been test escapes, some have resulted from design issues, and some have been customer production-line issues. Whatever the cause, we pull in a lot of experts to help our
customers solve their problems as quickly as possible."

What does Agere's ATE lineup look like? According to Matthias, "We've done a lot of work in
controlling costs internally over the last few years and have migrated from about seven different
ATE vendors down to primarily two—Agilent and Teradyne—although we still have some legacy
equipment." Why not standardize on just one? "We continue to look at that issue, but we believe
there is a healthy environment created by competition. So, not only from price perspective but also
from a technology perspective, we see a lot of benefit in driving a couple of vendors toward the same
goals." Some test development is done at remote locations, but most is done in the 31,000-ft²
Allentown test facility, where 35 ATE systems mirror the testers that Agere has deployed around the
world. More than 100 test engineers working for the various business units develop test programs.

Matthias added that there can be a downside to standardizing: "When you try to narrow down to a
very small number of providers, a lot of times you'll miss players in niche markets—for instance, one
that makes a very small, compact RF tester that does the job very well. It's a give and take—you
have to constantly keep looking at things. From a pure product-line perspective, it makes sense to go
out and pick the best equipment set for your particular product, and we were on that path in the
past, but from a manufacturing perspective and a support perspective, that's the most difficult thing
to do—you have to support all the interfacing, all the docking, and all the software for all these
different platforms, and it just becomes unmanageable very quickly."

Testing high-mix products

A particular challenge, Matthias said, is how to cost-effectively test high-mix products. "Many ATE
solutions involve changing pin cards in a test head. That approach might work well for a business
that has relatively few line items running at high volumes. But it doesn't work well for other
businesses that tend to have many more line items with different testing needs and lower-volume
line items. This week, I might need to test 30,000 parts from one product line, but then I might have
to take that tester off-line to switch out pin cards to reconfigure it for a different product that I need
to test next week. The end result is a lot of down time and a big hit on machine utilization. To
combat this, we try to deploy our equipment with a rather broad configuration that we can use for
many different product types." Sometimes, he said, this approach might complicate things like load-
board design, but it gives Agere a lot better equipment utilization in its factory.
He added, "DFT plays a big role in our strategy as we move away from the days of pure functional
test, where it could take a year to develop a test program." DFT and BIST, he said, enable rapid test-
program development and test-program conversions, allowing the company to quickly put a product
on a different platform to manage production spikes. "We are really trying to capitalize on the DFT
investment that we've made at the front end and take maximum advantage on the back end. We are
making a lot of progress there. It's a good news story for us."

Despite a streamlined tester lineup, ATE is still an expensive resource, and Matthias tries to avoid
tying up a system intended for production-test-program development to perform silicon debug or
failure analysis. To that end, he has enlisted benchtop systems from companies such as LogicVision
and Teseda for debug and other tasks (see "Failure analysis"). In particular, he noted that Agere has
used the LogicVision Validator to quickly bring up first silicon containing LogicVision BIST.

Of course, desktop debug units require a physical interface to a device under test (DUT), and using
such a unit can require a special debug load board in addition to a production load board. With such
boards costing $5000 to $10,000 and requiring a 5- to 8-week cycle time, that's a discouraging
prospect. To eliminate the need for a debug load board, Matthias employs production ATE boards
designed to facilitate use with the LogicVision Validator. The modified board employs various
connectors to provide access to power and ground planes, high-speed clocks, and the test access
port (TAP). It's been a tough sell to production-test personnel, he said, who don't care to see any
modifications that could conceivably interfere with production tests. To assuage their fears, he
employs high-speed relays to provide a clean path to the ATE and to switch out connector access
routes so the related load-board traces don't serve as stubs that could compromise measurement
results.

With the Validator, Matthias can perform debug as well as help with test-program development. For
example, he said he can experiment in real time with reordering tests to decide which ones to run in
parallel (which minimizes test time at the expense of potential power problems) and which to
perform serially (which minimizes power but extends test time).

The modified-load-board scheme works well with the minimal interface requirements of the
Validator, but it's not appropriate, Matthias said, for use with the Teseda V520, which requires a
high-density, 300-pin interface that Matthias doesn't believe is appropriate to add to a production
load board. For the Teseda box, a custom interface board is his preferred solution, although he
continues to experiment with designs for a generic solution that would take advantage of the
existing DUT card designs used for physical failure analysis at Agere.

**ATPG or BIST?**

While the LogicVision Validator box is designed to support BIST solutions, the Teseda box is
designed to support ATPG solutions, both of which are in wide-spread use at Agere, Matthias said,
adding that "from a test perspective, BIST is very attractive due to the small number of pins,
minimal ATE requirements, and built-in diagnostics. BIST is well-suited to lower-cost DFT-based
testers."

Nevertheless, some controversy swirls around the BIST vs. ATPG decision. See, for example, the
comments in favor of ATPG by Robert Hum, VP and GM of Mentor Graphics design verification and
test division (Ref. 2), and the response of LogicVision president & CEO Jim Healy (Ref. 3).

But neither Ternullo nor Matthias is dogmatic with regard to the issue, and both expect ATPG and
BIST approaches to find use. According to Ternullo, the optimum test solution for any product will
depend on the fault coverage it provides as well as on how well it is integrated with front-end EDA
tools and back-end debuggers and ATE systems. Ultimately, the choice will center on what best serves Agere's customers. Concluded Matthias, "At the end of the day, our number one goal is keeping the customer happy. Customer satisfaction is paramount."

**REFERENCES**