As semiconductor packages grow more complex, conventional continuity tests are no longer adequate for screening out open circuits and pin-to-pin shorts. Most test methods were designed for devices with pins aligned on the peripheral of the package. On today's micro surface-mount-device (SMD) and ball-grid-array (BGA) packages, however, the pins are aligned in a matrix—an arrangement that demands a new test approach.

In a typical continuity test, the test equipment applies a small current (usually a few milliamps) in parallel to all pins and measures diode turn-on voltage for each pin to verify continuity between the tester and the internal die. With the appropriate limit set for the expected diode-drop voltage for each pin, a single parallel continuity test can screen for parts with open I/Os.

Such a parallel continuity test can also detect shorted I/O pins, as long as the short causes the pin output voltage to swing away from a typical diode-drop voltage—for instance, to ground or to a high-
voltage state. But a parallel test is ineffective at catching a short that produces an insignificant voltage difference.

To screen for such shorts, you can employ other parametric or functional tests, but by using such an indirect method, you risk losing the ability to indirectly screen some shorted pins when production test steps become consolidated as a device matures. In addition, indirect continuity testing might not detect a short between devices where adjacent I/O pins do not exhibit significant functional differences, such as two output channels of separate but similar voltage regulators.

Obviously, you need to use a different method to guarantee that all tested parts are free from potential shorts between pins. The solution needs to take into account the complexity of matrix, or two-dimensional, I/O arrangements, without significantly increasing the test time and cost.

The matrix arrangement of today's package types significantly increases the probability of two or more pins being shorted together, as a pin in the center of the package could be shorted to any of the pins surrounding it. But doing a continuity short test on two adjacent I/O pins for every combination would be counterproductive, especially as the I/O count increases.

**The black & white continuity test**

One method that shows promise for using ATE to detect opens and shorts without sacrificing test efficiency is a technique that I call the “black & white” continuity test. The black & white continuity test attempts to use a minimal set of test conditions to detect all potential shorts between two or more pins on a package.

In conventional pin-to-pin continuity test, the test iteration depends on the I/O count. For an I/O matrix of \( m \times n \) where \( m \) is the number of rows and \( n \) is the number of columns, it takes \((m \times n) - 1\) iterations to detect all potential shorts.

For typical ATE, the continuity test alone can take 1 s or more when the I/O count exceeds 100. The black & white test method, however, can hold continuity test time to tens of milliseconds, regardless of the number of I/O pins. The only additional test time required for this method involves tests needed for pins that cannot be toggled to ground.

In the configuration shown in **Figure 1a**, a short between two adjacent pins can occur in many different ways. For each fully surrounded pin (such as the red pin in **Figure 1b**), there are at least eight possible ways for a short to occur.

![Diagram](image)

Figure 1. (a) A grid arrangement provides many possibilities for pin-to-pin shorts. (b) The red pin could be shorted to any of the eight pink pins. (c) Black I/O pins are grounded, while the white I/O pins are tested for continuity. A test setup can detect horizontal and diagonal shorts between I/O pins. (d) Reversing the black and white I/O setups enables detection of vertical shorts.

A lengthy way to ensure that ATE can detect each possible short is to force a ground potential across all the pink I/O pins and test the red I/O for continuity. Should a short occur, the tester would
measure a ground voltage instead of a diode turn-on voltage on the red pin. This process would have to be repeated for the rest of the I/O pins to fully cover all the possibilities—clearly not an efficient option for high-pin-count devices.

The black & white continuity test method—derived from a checkerboard pattern—is more efficient. To fully test every pin for opens or shorts to adjacent pins, the black & white test method requires only three continuity test iterations, regardless of the number of I/O pins available on the package. It is applicable to all matrix-type packages, including micro SMD and BGA, and is even applicable to multi-row and multi-column in-line packages like high-pin-count leadless lead-frame packages (LLP).

The first continuity test iteration tests for opens on all of the pins in parallel. If any pin has an open circuit, it fails this test. In the second setup iteration (Figure 1c), the ATE drives black pins to ground to test the white pins. This test detects shorts occurring between diagonally or horizontally adjacent pins, but it will not detect shorts between vertically adjacent pins. The third iteration (Figure 1d) handles that final case.

Although the black & white test method attempts to reduce the number of iterations to three, situations inevitably arise that demand more iterations for complete coverage. One such situation arises because of supply and ground I/O pins. Another is mainly caused by the way the test hardware accesses the DUT (see "Test hardware design," p. 42).

![Figure 2. (a) This 16 I/O pin configuration has multiple supply (red) and ground (blue) I/O pins. (b) Ground potential (black) is established at the device ground I/O pins, and continuity is measured on all white (nonadjacent) and yellow (adjacent) pins.](image)

**Multiple supplies and grounds**

For supply pins, it’s common to use a supply-current test to guarantee continuity. Grounds, on the other hand, are commonly used as the reference for continuity testing. Some designs discourage forcing grounds to a potential higher than other I/O pins, as this could reverse-bias some circuits and damage the die. Therefore, testing supply pins and grounds for opens and shorts requires some planning.

Consider the I/O configuration shown in Figure 2a, where the red I/O pins are supplies and the blue I/O pins are grounds. To test for continuity, you must first identify which I/O pins are supplies and grounds and then apply the black & white steps. First, test for opens on all pins in parallel. Then, force ground pins to ground potential. Note that any short between ground pins and their adjacent
pins (yellow) would cause the continuity test to fail (Figure 2b).

Next, establish ground potential on alternate columns and measure continuity on remaining pins (Figure 3a). As the device supplies and grounds are usually connected together on the die, the effective configuration would appear as shown in Figure 3b. This second iteration can detect all horizontal and diagonal shorts on all white I/O pins. For a few combinations, however, detections are not possible. Horizontally and diagonally adjacent pins that cannot be detected for shorts are shown in green in Figure 3c.

![Figure 3](image)

Figure 3. (a) Black pins are grounded while white I/O pins are tested for continuity. Red and blue pins are effectively grounded because of internal die connections and are shown in black in (b). The green pins in (c) represent undetectable shorts.

The next iteration detects vertical shorts by switching the vertical black (grounded) I/O pins to horizontal (Figure 4a). For continuity testing, at least one device ground is set to ground potential. Again, because supplies and grounds on the die are commonly connected, the resultant configuration is as shown in Figure 4b. To check for non-testable pins, scan vertically for pins under test that do not fall next to a black pin in the same column. These non-testable pins are highlighted in green in Figure 4c.

![Figure 4](image)

Figure 4. (a) The horizontal ground configuration can detect vertical shorts. (b) This figure shows the effective configuration with commonly connected device supply and ground I/O pins. (c) Pins shown in green are undetectable for shorts in the vertical direction.

Performing an AND operation (Figure 5a) on all green I/O pins in Figures 3c and 4c can check for any pin that cannot be tested for a short. All black and green pins are treated as logic 1, while all white pins are treated as logic 0. (Note that if two corresponding pins are black, the results of the AND operation can be ignored since both of these I/O pins could be detected for shorts in the first place. These I/O pins are redundant in this analysis.)
Finally, apply an exclusive-OR (XOR) operation between the output from the logic AND operation (Figure 5b) and the parallel continuity test configuration from Figure 2b. The final iteration to test for pin-to-pin shorts is now to set the device supplies and grounds to ground potential and then test for continuity on the remaining pins with undetectable shorts (Figure 6).

Here, a four-iteration continuity test is sufficient to detect all possible shorts between two adjacent pins compared to 15 iterations for a thorough per-pin continuity check. View a table that summarizes these steps.