How software enhances boundary scan

Rick Nelson - March 01, 2003

Boundary scan is becoming indispensable to the cost-effective production of dense PCBs. Boundary-scan implementation begins with the software that helps you design boundary-scan-compatible PCBs and develop the test vectors that your lab and production equipment will use to exercise them.

Boundary-scan software plays a role in the development environment, in run-time production test, and in field service. Complementing the basic boundary-scan software are tools that provide such capabilities as schematic viewing or test-coverage analysis.

Boundary scan's goal is to provide input vectors to a product under test via a minimum number of test I/O lines—ideally the four lines (clock, data in, data out, and test mode select) defined in the IEEE 1149.1 standard (Ref. 1). The technology also evaluates the corresponding output vectors. A variety of hardware options—from stand-alone boundary-scan controllers to production-floor in-circuit testers (Ref. 2)—can generate and acquire those signals, but software determines what values those signals should take.

Boundary-scan design flow

A typical boundary-scan design begins with a parts list containing boundary-scan-compliant as well as non-compliant devices. The compliant devices come with boundary-scan description language (BSDL) files that describe their behavior with respect to boundary-scan Test Access Port (TAP) inputs and outputs. These files, along with board schematic information from PCB electronic-design-automation (EDA) tools, serve as the input to boundary-scan development software tools, such as Acculogic's ScanManager, Asset InterTech's ScanWorks, Corelis's ScanPlusTPG, Goepel Electronic's...
System Cascon, Intellitech's Eclipse Test Development Environment, and Teradyne's Victory.

Those tools develop the patterns necessary to test boundary-scan devices and configure in-syste-
-programmable devices. In addition, they can suggest test strategies for clusters of non-boundar-
-scan-compliant devices, determine fault coverage, and suggest possible test-point additions that
extend fault coverage at minimal cost.

Thomas Wenzel, vice president at Goepel Electronic (Jena, Germany), says that when choosing
boundary-scan tools, customers typically evaluate software first. Only in applications requiring high-
speed flash programming (Ref. 3) do they think of hardware first. He recommends a fully integrated
boundary-scan development environment (incorporating a frame structure with plug-ins), such as his
firm's System Cascon, in place of a combination of stand-alone tools.

Dave Bonnett, technical marketing manager at Asset InterTech, emphasizes that it's important for
prospective customers to look beyond their immediate needs: "First time or inexperienced users
usually have a very focused view of a boundary-scan system. They are cost-sensitive, and they want
to know if the system will solve a particular problem that they are currently facing."

In contrast, Bonnett adds, experienced users are more concerned about the broad capabilities of the
boundary-scan system under consideration and whether it can effectively integrate with other
processes and procedures. The more mature user usually wants to know how tests and programming
operations generated by a boundary-scan system will support prototype debug, as well as how they
will work with in-circuit test, functional test, BIST (built-in self-test), and other types of test. Says
Bonnett: "One of [Asset InterTech's] ScanWorks' strengths is its ability to enable test re-use." This
extends from design and development into manufacturing as well as environmental-chamber and
other types of testing.

Menachem Blasberg, president of Corelis, agrees that an effective boundary-scan system should
work well with other test and development tools you have in place. What's nice about Corelis
software, as well as its competitors' software, he contends, is that you can call and execute
boundary-scan tests from other programs such as LabView, Agilent Vee, and custom test executives.
That can facilitate testing for customers who decide to forgo in-circuit test in favor of coupling
functional tests developed within LabView, for example, with boundary-scan tests.

From DC test to ISP

Originally conceived as a low-speed or DC interconnect test standard, IEEE 1149.1 has yielded new
standards (Refs. 4, 5, and 6). Those new standards define the programming of onboard flash
memory. In addition, one of those standards—IEEE 1582—defines the configuration (or field
reconfiguration) of in-system-programmable (ISP) field-programmable gate arrays (FPGAs) and
programmable logic devices (PLDs).

From product development to field service, boundary-scan software offerings cover a wide price-
-and-performance spectrum. Products range from less-than-$1000 versions offering only low-speed
IEEE 1149.1 test to $50,000 systems that offer DC test and AC test as well as flash programming
and programmable-device configuration in accordance with IEEE 1582 and other emerging specs,
plus such bells and whistles as schematic viewers (Figure 1) and test-coverage analyzers.

A typical high-end software package is Corelis's ScanPlusDFT, which, according to Blasberg, can
evaluate boards and systems that include a mix of boundary-scan and non-boundary-scan devices.
ScanPlusDFT reports test coverage of every net and pin on the board and indicates whether a net or
pin is fully testable, partially testable, or nontestable. It suggests where test points can be added to
enhance testability while reducing the need for nails in in-circuit-test fixtures. Another feature—Corelis's support for testing embedded cores in semiconductor devices—has earned Corelis "LogicVision Ready" status. This means Corelis has demonstrated that its tools support tests of ICs containing LogicVision embedded-test intellectual property (IP).

**Test effectiveness**

Ray Dellecker, US marketing manager at JTAG Technologies, notes that if he had to select one issue that has a major impact on the overall effectiveness of boundary scan, it would be the quality and capabilities of the test-development software. He adds that software can provide high levels of automation, but the software's test generator must do a thorough and reliable job, evaluating all possible nets and conditions. "Our software tools achieve a balance between pushbutton operation and verification of the designer's intent," says Dellecker. "Other factors, such as board design, BSDL quality, and links to the EDA system, are becoming much more manageable these days as the industry has matured."

Corelis's Blasberg notes that poor-quality BSDL files have been a main restraint on boundary-scan's effectiveness, but he agrees that BSDL problems have been drastically reduced in the past couple of years. Matt Van Wagner, director of sales and marketing at Flynn Systems, attributes BSDL improvements in part to the efforts of Agilent Technologies' Kenneth Parker, who helped establish a free Web-based automated BSDL syntax checker ([www.ate.agilent.com/emt/library/smart_tools/verification](http://www.ate.agilent.com/emt/library/smart_tools/verification)).

Improvements in BSDL files leave other factors to determine overall effectiveness of boundary-scan implementations. Wenzel at Goepel Electronic cites such factors as the performance of a chosen boundary-scan system and the skill of the design and test engineers who develop boundary-scan-enabled PCBs and their test procedures. Bonnett at Asset InterTech agrees: "The main determinant in the effectiveness of boundary-scan test is the quality of the design-for-test (DFT) practices followed by the development group. Unfortunately, no boundary-scan software system can overcome DFT deficiencies."

Tom Jackson, director of marketing and sales at Intellitech, elaborates: "There is a misconception in the market, caused by some of the vendors themselves, that IEEE 1149.1 tools are not sophisticated and do not require technical expertise to evaluate. This is not the truth. DFT . . . is a global design issue and must be treated as such. Today, DFT means much more than daisy-chaining ICs in the 1149.1 chain."

To that end, says Jackson, Intellitech provides infrastructure IP to system designers to help them implement effective strategies for embedded configuration and test. The company's patent-pending IP "provides a scalable configuration, debug, and test infrastructure that enables customers to build self-testable and in-the-field reconfigurable products." The company's products include SystemBIST IP, a plug-and-play IP module that enables IEEE 1532-compliant in-system configuration and IEEE 1149.1 test; FAC IP, an IP module that programs flash memory in-system at maximum speed; and Scan Ring Linker IP, which links multiple scan rings (secondary scan paths) into a single high-speed test bus, permitting devices on secondary scan chains to be independently tested and configured through a single IEEE 1149.1 external interface.

Says Bonnett at Asset InterTech, "Each boundary-scan tool vendor has unique test-generation tools with vendor-specific methods of applying the tests and diagnosing the results." Vectors developed on one vendor's platform, he said, can be transported to another vendor's platform by using industry-standard Serial Vector Format (SVF) files, but diagnostics on alternative platforms is generally
limited to pass/fail. Apart from the SVF standard, Asset for its part has pursued seamless integration with Agilent Technologies' 3070 in-circuit test systems and with Teradyne's Victory boundary-scan software. Wenzel at Goepel noted that PLD formats such as Jam STAPL (see "Glossary," p. 28) can complement SVF for effective transfer of boundary-scan data among diverse platforms.

**The price is right**

Dellecker at JTAG Technologies puts the typical capital investment for boundary-scan testing at 10% to 20% of the investment required for traditional testing. Nevertheless, some see the cost of boundary-scan test as still too high. In an alliance formed to make JTAG testing more affordable to mainstream test and design engineers, Ricreations and Flynn Systems announced last November that they will jointly market their sub-$1000 Universal Scan and onTAP boundary-scan-test software packages. Ricreation's Universal Scan focuses on manual debugging of JTAG scan chains and circuits; Flynn Systems' onTAP provides ATPG for full automated board test.

Says Flynn's Van Wagner, "Hardware designers are vitally important to the implementation of boundary-scan DFT. The more affordable boundary-scan tools are, the more likely hardware designers are to use them. These designers are much more likely to consider tools that are under $1000 than tools that cost $10,000 to $50,000."

**For more information**


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### Manufacturers of boundary-scan software

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<tr>
<th>Company</th>
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**References**