Test-failure data contains a wealth of information that can accelerate the yield-analysis process for semiconductor devices. By setting up an infrastructure that captures and automatically diagnoses each manufacturing test failure, you can create a valuable database of information based on actual silicon results. When you couple this database with a diagnosis-driven yield-analysis tool that performs statistical analysis on this large volume of diagnosis data, you can significantly reduce the time needed to recognize systematic yield issues and determine their root causes.

The role of scan diagnosis

A key goal in the yield-analysis process is to identify the root cause of yield loss. The most significant challenges include:

- separating devices with systematic issues from those with random defects,
- identifying fail-mode similarities across multiple failing die, and
- localizing and identifying physical defects.

Scan diagnosis is an established software-based method for defect localization and is used as part of the failure-analysis process (see “Yield challenges and traditional tools for semiconductor companies”). Scan diagnosis identifies the location and classification of a defect on a die based on the design description, the test patterns used to detect the failure, and the failure data from the tester. A scan-diagnosis tool will typically process each failing die individually. For each defect on each die, the diagnosis tool will output a list of “suspects;” that is, suspected defect locations and mechanisms.

The quality of a diagnosis result is typically measured by accuracy and resolution. A diagnosis result is accurate if the actual defect location is in the list of suspects that the diagnosis tool generates. The resolution of the result is determined by the number of suspects in the list and by the physical area where the suspects reside. For instance, the tool may provide a suspect list of 10 nets, while the actual defect affects just one of these 10. A higher resolution tool would provide only one net or, even better, just a segment of the net where the actual defect is located.

Extending the role of diagnosis

To address the first two challenges listed above—separating devices exhibiting systematic issues from those with random defects, and identifying fail-mode similarities across multiple failing
die—you must select the right devices for failure analysis. This selection has traditionally been done without the aid of diagnosis, and it may be a trivial task if the presence of a systematic issue is obvious. For example, if all but one wafer has zero defects, and this one wafer has 100 failing die that are all in the center of the wafer, you can assume with relative certainty that all these die fail for the same reason. No matter which die you pick for failure analysis, the die will represent the root cause.

But at very small process nodes, a combination of effects can easily mask systematic issues and produce failure patterns on a wafer map that appear random. In these situations, you need tools that examine diagnosis data from large numbers of die in order to recognize patterns in the data that point to systematic causes. Such diagnosis-driven yield-analysis tools use statistical techniques to recognize correlations based on many different factors, helping to point you to views of the data that have meaningful information.

Consider a hypothetical example where most wafers have 50 failing die, but one wafer has 100 failing die. If you randomly pick one die for failure analysis from the excursion wafer, you have only a 50:50 chance that the selected die has a defect related to the increased fall-out on that particular wafer. In other words, it can be hard to distinguish between systematic and random issues, especially if multiple systematic issues are hidden in the data. Chances are that when selecting devices for failure analysis, you will end up with devices that failed for different reasons.

![Figure 1](image.png)

**Figure 1.** A diagnosis-driven yield-analysis flow can increase your chances of picking the right die for failure analysis. The failure-localization step, which includes diagnostic automatic test-pattern generation and physical-fault isolation, is optional.

To increase your chances of picking the right die for failure analysis, you can use scan diagnosis to look for patterns across a large number of failed die by integrating a volume diagnosis step into your testing and yield-analysis process (Figure 1). In a traditional flow, scan diagnosis is not used until the physical-failure-localization step, which is done before construction analysis. In a diagnosis-driven yield-analysis flow, you can employ scan diagnosis earlier to help select the correct die and thus eliminate the costly physical-failure localization step.
The diagnosis-driven yield-analysis tool will classify the results of the scan diagnosis into categories such as defect mechanism, cell type, logic, and physical locations. This classification step enables you to separate the die into correlating categories such as defects in different instantiations of a particular standard cell or defects involving a particular type of via.

**Effectively using volume diagnosis results**

What ultimately determines the value of diagnosis in yield analysis is how the diagnosis results are used. To effectively leverage diagnosis results, you need to separate systematic issues from noise (Refs. 1, 2, 3). You can approach this in several ways.

In the case of a typical yield excursion, yield loss is easily observable. To get to the root cause in such a case, you would group devices with common failure features and then select those devices with the most representative, highest-resolution diagnosis results for failure analysis.

For example, consider the hypothetical case of an excursion wafer that has 250 failing devices, 150 with suspected bridge defects. Of these 150 die, 120 have bridges in the metal2 layer. Of the 120, there are 50 with just a single diagnosis suspect, and out of this subset, 20 have high-resolution results. By leveraging diagnosis data in this way, you can find the suspected systematic defect mechanism (bridge in metal2) before failure analysis and select a device that clearly exhibits this behavior. Then, you can skip the costly physical-localization step and go straight to construction analysis.

![Figure 2. (left) A visible pattern may not be evident from a stacked wafer map of all failing die, but you can use zonal analysis to separate systematic defects from random issues. (right) Die corresponding to the upper left corner of the reticle failed systematically.](image-url)

In other cases, when multiple issues are present, separating random from systematic issues may be challenging. When you look at a stacked wafer map of all failing die, a visible pattern might not be evident, as shown in the left wafer map in Figure 2. To determine the presence of systematic failures, you could randomly select a large number of devices for diagnosis and failure analysis and hope that many would exhibit the same failure. This approach is costly and time-consuming.

A different approach involves diagnosis followed by identification of the most variant failure features. For instance, while the distribution of failing die may appear to be random, the distribution of die with one particular diagnosis signature, such as devices failing for one particular type of standard cell, may be systematic in nature; as shown in the right wafer map in Figure 2. The pattern shown in this example indicates that the die representing the upper left corner of the reticle failed systematically. This information is useful in determining the root cause.
The technique used here is called “zonal analysis” and is used in the Tessent YieldInsight tool from Mentor Graphics (Figure 3). It is one of many possible correlation techniques. With zonal analysis, the tool automatically examines the various diagnosis signatures of many failing die and flags those that have an unexpected distribution across the data set. Another technique is to correlate failures with DFM (design for manufacturing) violations. No matter which cross-correlation technique is used, the intent is to separate the valuable results from the noise.

**Figure 3.** Scan diagnosis as performed by the Mentor Graphics Tessent Diagnosis tool makes use of design, test-pattern, and ATE fail-log input data; the tool then outputs defect classification, logic location, and physical location.

**Practical requirements for volume scan diagnosis**

To use a diagnosis-driven yield-analysis flow, you need to manage the process of collecting failure data from multiple test systems and automatically performing volume scan diagnosis. One factor that makes this challenging is that different ATE (automated test equipment) platforms have different capabilities in terms of how much data they collect and how well they collect it. Besides this, two other factors complicate the collection of logic test failures: the lack of data-log format standards, and the lack of ATE operating system features that support failure-log data collection.

Consequently, to be able to implement volume scan diagnosis, you have to ensure that failures are correctly logged with robust data-traceability features. And you’ll want to do this in a way that minimizes the impact on test quality, test throughput, and tester and computational resources.

Most semiconductor companies use a combination of stuck-at and at-speed test patterns. The majority of defects may fail both of these pattern sets, but diagnosing at-speed patterns requires more effort, because they are typically more complex and longer than stuck-at patterns. In addition, one particular defect mechanism may cause failures in the functional circuitry for some devices and in the scan chains themselves for other devices, but diagnosing scan-chain defects requires significantly more data than diagnosing failures in the functional circuitry.

In general, the more fail data that is collected, whether scan or functional, the better the diagnosis result. You can still perform an effective diagnosis with a relatively small amount of fail data per die. This is important, because in many cases, it is not practical to collect data from and perform diagnosis on all failing die. The minimum number of die needed depends on the type of issue to be analyzed.

For instance, the analysis of an excursion has different requirements compared to identification of a hidden yield limiter. As a sample calculation, assume a known systematic signature has been responsible for 5% of yield loss. To have a statistically significant sample, you may need at least 25 die that have this signature. Thus, data will be needed to be collected on 500 die (that is, 25 divided by 0.05).

**Example application of diagnosis-driven yield analysis**
Diagnosis-driven yield analysis is particularly relevant during two situations: a new technology introduction, and a new product introduction. In both cases, critical issues affecting yield are common. You may need to simultaneously explore multiple sources of the root cause of failures.

At STMicroelectronics, we dealt with a scenario that combined both a new process technology and a new product. Since the early maturity phases, both the yield data for the TC (test chip) and the yield and diagnosis information for the final product, an SOC (system on chip), were available. The yield of the TC and SOC were different despite the designs being comparable in size. A possible explanation for the difference resided in the different architectural and topological complexity of the two designs.

TCs are designed to explore yield performances of different layout configurations and to validate IP libraries. They typically have regular structures such as RAM and ROM or cell arrays. They also include ring oscillators and arrays of combinatorial and sequential logic cells. Electrical activation is made as simple as possible to reduce the variables that would have to be considered during the analysis of the test results.

On the other hand, end-product SOCs are irregular structures, in which the electrical activation complexity depends on many factors driven by functional requirements. The structural differences between TCs and SOC products with respect to electrical activation provide critical information that can be applied to yield analysis.

In the early phases of a new technology introduction, several defect sources may be aliasing each other. The observed failures may therefore indicate a different defect mechanism than those actually causing the failures. This was exactly the case we faced with the yield gap that existed between the STMicroelectronics TC and SOC products.

The first analysis action we took was to verify if and how the yield was affected by any type of systematic marginality that was dependent on the SOC implementation. The dependencies could have been timing-critical paths, crosstalk effects between adjacent wires, or power limitations. We used volume scan diagnosis to help verify design-related systematic effects.

We expected that the failure signature would also include evidence of the problem. The simple cumulative analysis of the failure signature could indicate the presence of the systematic problem, and the cumulative analysis of the diagnosis results would allow us to find the fault location with a better resolution.

In our case, no symptoms were present that indicated design issues. Consequently, we proceeded to filter out from the diagnosis results all signatures of a random nature. To do this, we used the TC information as well as comparative analysis across multiple sets of material.
For our second step, we employed zonal-analysis techniques to isolate the signatures that were present. We observed two combined factors: a deterioration of performance moving from wafer border to center (Figure 4), and a similar, emphasized behavior exhibited by some core library cells. By analyzing the layout of the library cells that exhibited the deteriorated performance, we were able to determine whether the defects occurred in the same relative location and to guess the possible criticalities associated with them.

The third step was to select a few die across the many that showed a similar signature, where confidence on symptoms was higher. In addition to the die exhibiting the systematic issue, we also selected die that were classified as affected by a random defect in order to confirm the presence of physical defects not of a systematic nature (Figure 5). Our physical analysis confirmed that the marginality on performance was caused by an improper process centering.

The fourth and final step, in parallel to tuning the manufacturing process, was to continue to observe the failure signature trend. This was done to verify that the critical signature was becoming negligible as a result of the process tuning.
Where does diagnosis-driven yield analysis fit?

A yield-analysis flow based on scan diagnosis is not meant to replace all the other yield-improvement techniques that are in use. Rather, it supplements established techniques. A yield-management system continuously monitors data from multiple sources and provides a high-level view, quickly informing if something is going awry.

Diagnosis-driven yield analysis involves deeply diving into both the design and test failure data of the specific device, rather than only relying on manufacturing process data. Consequently, it can often provide more specific information to guide the physical failure-analysis step, and it can help uncover design-related systematic issues that are difficult to discover using process data alone.

Diagnosis data collected in volume can also be exploited for monitoring purposes, as a shift in the process performances may lead to a variation in the electrical signature. Thus, diagnosis should be added to the other traditional instruments used for yield analysis to reveal the effect that defects have on the electrical behavior of the SOC.

While yield analysis has traditionally been an issue for IDMs (integrated device manufacturers) and foundries, sometimes fabless semiconductor companies need the ability to analyze yield. A diagnosis-driven approach may be suitable in these cases, because the focus is on test results rather than manufacturing results.

Diagnosis-driven yield analysis can also be used to improve the effectiveness of DFM rules by correlating actual root causes to rules employed during verification and setting higher priorities for those rules that would mitigate the types of failures experienced. In this way, design sensitivities are uncovered to drive yield learning across many designs at a particular process node. This is also important in a foundry environment where many designs may be sharing the same manufacturing line.

References