Mentor Graphics and ARM team up on memory test and repair

Rick Nelson - November 06, 2010

Mentor Graphics at the International Test Conference highlighted its announcement that it has teamed up with ARM to provide an automated memory test and repair capability for ARM embedded memories and processor cores. The new capability provides interoperability between Mentor's Tessent memory test and repair product and ARM's family of cores and embedded memory IP.

"The requirements for embedded memories are increasing as design complexity and demand for feature rich functionality grow," said Simon Segars, executive VP and GM of the ARM physical IP division, in a press release. "An effective memory test and repair solution is critical to ensuring high quality levels and maximum product yield. We are pleased to be working with Mentor to ensure a robust memory test and repair solution is available to our mutual customers."

ARM now includes an optimized memory BIST bus and interface that provides external access to all memories contained within the processor core. This integrated feature enables normally intrusive memory BIST IP to be placed outside the core, removing any impact to processor performance. Mentor's recently introduced Tessent memory BIST and self-repair solution has been enhanced to fully support this interface. The Tessent MemoryBIST product automatically configures, generates and integrates memory BIST and self-repair IP that operates with an ARM processor core's specific bus and embedded memories.

The Tessent solution also supports ARM memory compiler features. ARM has developed the capability to generate a complete Tessent memory view for memory instances generated by their compilers supporting TSMC 40nm and Common Platform 32- and 28-nm processes. This interoperability enables an automated flow for adding Tessent test and repair functionality to ARM embedded memories contained anywhere within a design or processor core.

"With the huge complexity involved in testing the latest processor-based SoCs, designers need as much automation as possible to ensure that testing does not become the bottleneck in getting new designs to market," said Joseph Sawicki, VP and GM for the design-to-silicon division at Mentor Graphics, in a press release. "At the same time, they cannot afford to skimp on the quality of test. This integration between Tessent and ARM technologies gives customers what they need to deliver the most advanced, defect-free IC products to market in a timely manner."

The Tessent memory test and repair tool is only one facet of Mentor's efforts to address emerging silicon test challenges, said Greg Aldrich, marketing director at Mentor, in an interview at the International Test Conference. To help designers contend with new manufacturing processes, larger designs, whole-chip test-management issues, shrinking product windows, and 3-D test issues, Aldrich said, Mentor provides four key families in the Tessent product line:
· digital logic test (Tessent TestKompress, FastScan, LogicBIST, SoCScan/DFTAdvisor, BoundaryScan),

· mixed-signal high-speed I/O (Tessent PLLTest and SerDesTest),

· embedded-memory test (Tessent MemoryBIST), and

· silicon learning (Tessent SiliconInsight, Diagnosis, and YieldInsight).

Mentor's test lineup, Aldrich said, has allowed the company to capture 54% market share for 2009, according to EDAC 2010 figures.
