In January 1979, *Electronic Test* published an article claiming that a single test circuit that could "perform all the standard DC tests needed to thoroughly check any kind of operational amplifier" (Ref. 1). At that time, a single test circuit may have been sufficient, but not today because modern op amps have far better specs. Thus, a single test circuit no longer covers all DC measurements.

Today, three test-circuit topologies are commonly used for bench and production testing of DC parameters in operational amplifiers. These three topologies are 1) the two-operational-amplifier test loop, 2) the self-test loop, sometimes called a false-summing junction test loop, and 3) the three op-amp loop. You can use these circuits to test DC test parameters that include $I_Q$ (quiescent current), $V_{OS}$ (voltage offset), PSRR (power supply rejection ratio), CMRR (common-mode rejection ratio), and $A_{OL}$ (DC open-loop gain).

**Quiescent current**

Quiescent current is the current a device draws with its output current equal to zero. Although an $I_Q$ test may seem rather simple, you must take care to ensure good results, especially when dealing with either very high or very low $I_Q$ parts. **Figure 1** shows the three practical circuits that can be used to test $I_Q$ and the other parameters, but it is essential to consider any load currents. This includes feedback current in the test loop. The feedback resistor $R_f$ actually can put a load on the part that can affect the $I_Q$ measurement.
To show you an example of these circuits, we tested the OPA369 op amp. The maximum quiescent current for this part is 1-µA per channel. The maximum input offset voltage is 750 µV. The two-amp-loop circuit in Figure 1 puts a voltage of 750.75 mV on the output of the DUT (device under test). That input voltage puts 15 µA through $R_f$. This current comes from the power supplies and it will add error to any measurement. Therefore, you must take steps to ensure that the output current is truly zero before making the $I_Q$ measurement.

The self-test circuit isn't the most efficient circuit for measuring very low quiescent currents because of the feedback current that the output must provide. In this implementation, the output must be adjusted to the gained-up voltage offset $V_{OS}$—not always an easy task—or the 50-Ω resistor in the above schematic would need to be switched out to eliminate feedback current. The two-amp loop accomplishes the zero output requirement by adding another amplifier. By carefully choosing a low-input bias current loop amp, the output current should cause an insignificant error.

The three-op-amp loop also lets you measure $I_Q$, but take care because of the 1-MΩ resistor at the DUT's output, which becomes an issue because it's always a parasitic load, regardless of which parameter you're measuring. If you're measuring output load current, then this resistor represents an additional load. You must also consider the resistor noise, which is 85 μV peak-to-peak (p-p) from 0.1 Hz to 10 kHz for the 1-MΩ resistor. Using a 100-kΩ resistor would reduce the noise to 27 μV p-p. So, you can drop the resistor value to reduce noise, but then the parasitic resistor loading on the output of
the DUT is more significant.

Voltage offset

The $V_{os}$ test is fundamental to the measurement of most other op amp DC specifications. Therefore, pay careful attention to the test circuit, making sure that it also works well when testing all other parameters. Poor choices in the configuration of this test can compromise the other DC measurements.

$V_{os}$ is defined in different ways. A few standouts include "the differential DC input voltage required to provide zero output voltage with no input signal or source resistance," (Ref. 2) or "the differential DC input voltage require to provide zero output voltage, with no other input signal and zero resistance in either input terminal path to ground," (Ref. 3). Another definition, "the differential DC input voltage required to provide zero voltage at the output of an operational amplifier when the input bias current is zero" is an ideal theoretical method for testing the input offset voltage, which isn't practical because no op amp has zero input bias current.

The definitions suggest that you connect a low output, high accuracy, fine resolution variable voltage source to the input of the op amp and adjust the input voltage until the output voltage is zero. Then, the input offset voltage would simply be the inverse of the input voltage applied.

There are two serious problems with this method. When testing op amps with very high open-loop gain, you must make sure that the voltage source's resolution is less than a microvolt to guarantee any degree of repeatability. You must also use an iterative approach drive the output to zero. Noise in the system, coupling into the voltage source and op amp, makes the measurement and control next to impossible in a high-speed automated test environment.

Given the problems with the ideal method, the usual method of choice in bench test environments is to put the DUT in an inverting gain configuration as shown in Figure 2. This method has an advantage in that the DUT is stable and no additional compensation is usually required.

Test circuits may also include a 50-Ω resistor between the noninverting input and ground for input-bias current cancellation. But, with very low input-bias-current op amps, the only real contribution of this resistor is additional noise. For a 100-pA part, the additional error without this resistor is only 0.005 µV. This cancellation only works if the bias currents are equal in direction and in magnitude.

The circuit in Figure 2 is a simplification of the self-test summing junction method in Figure 1, but...
without resistors $R_1$ and $R_2$. This circuit is also inherently stable for most op amps, which often outweighs any of the potential disadvantages and makes it the preferred test circuit.

The disadvantages of using the test circuit in Figure 2 present themselves if you choose to use it to perform additional testing. For example, the circuit in Figure 2 has implications for testing other parameters such as $I_Q$ and $A_{OL}$.

This circuit, left undriven, results in a $V_{OS}$ error equal to $(V_{OS} \times \text{closed loop gain}) \times A_{OL}$ in V/V. This error may be insignificant, or may be reduced by driving $V_{OUT}$ to 0.0 V by applying the appropriate $V_{IN}$.

The equation used to compensate for the error at the output from the desired output can be adjusted using the following calculation Equation 1.

$$V_{OUT} = (2 \times A_{SJ} + A_{CL} - A_{SJ}) \times V_{OUT \text{ (ideal)}}$$  \hspace{1cm} (Equation 1)

where $A_{SJ}$ is the summing junction gain, and $A_{CL}$ is the closed loop gain.

Often, an additional amplifier is used in the test loop, as shown in the two-amplifier loop in Figure 1. This configuration comes closest to meeting the definition for $V_{OS}$. The DUT's output is held within the $V_{OS}$ of the loop amplifier to ground. You can null out the offset of the loop amplifier if it has a $V_{OS}$ adjustment or you can control the noninverting input to eliminate the offset. In this way, you can drive the output of the DUT to zero. The voltage measured at $V_{OUT}$ is $1001 \times V_{OS}$. Unless a load is attached to the DUT's output, the output must only supply the input bias current of the loop amplifier. This is an important consideration for low $I_Q$ parts when measuring quiescent current. In the previous two circuits, the DUT must supply the feedback current into $R_f$.

By connecting the noninverting input of the loop amplifier to a programmable voltage source, you can make many other op amp performance measurements such as $A_{OL}$, output swing, and CMRR. As the loop control voltage is varied, the output of the DUT attempts to match the control voltage.

Note the following disadvantages of a two-amp loop:

- Additional complexity as opposed to the self-test circuit.
- Loop compensation is required because the circuit isn't inherently stable.
- The output of the DUT can be controlled only over the loop amplifier's common-mode range.

The circuit will oscillate if the loop isn't properly compensated. You can stabilize the loop by placing an appropriate capacitor in parallel with $R_v$. Placing an appropriate RC combination across the loop amplifier will also stabilize the loop. We will discuss compensation of this loop in a future article.

A variation on the two-amplifier loop test method is the three-amplifier loop, which uses current steering for DUT output voltage control. The compensation for this loop is set by the RC combination across the second loop amplifier. As in the two-op-amp circuit, the voltage offset of the DUT is measured at $V_{OUT}$, and $V_{OUT}$ is 1001 times the voltage offset. This topology solves the DUT output swing limitation of the previous circuit. If greater output swings are required, the resistor in series with the loop control voltage can be made smaller.

Note the following disadvantages to the three-amplifier loop.
• Additional complexity compared to the other circuits.
• Loop compensation is required. It is not inherently stable.
• The output of the DUT always has a minimum 1-MΩ load.

Power supply rejection ratio

PSRR is the ratio of the absolute value of the change in power-supply voltages divided by an op amp's change in the input-offset voltage. Simply put, it's the op amp's ability to reject changes in the power-supply voltages over a specified range. Because you need the offset voltage to make this measurement, you can use the techniques already developed for measuring $V_{os}$. Any of the three test loops in Figure 1 will work for PSRR measurements by setting the power supplies, $+V_S$ and $-V_S$, to the minimum supply voltage for the DUT and measuring $1001*V_{os}$. Next, set the power supplies to the DUT's maximum voltage, then measure $1001*V_{os}$ again. Equations 2 and 3 show how to calculate PSRR.

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{os}}$$

Equation 2

$$PSRR(dB) = 20\times\log\left(\frac{\Delta V_{supply}}{\Delta V_{os}}\right)$$

Equation 3

Some op amps require additional considerations when using this method. These op amps have a low enough operating voltage that the mid-point of the power supplies (zero common mode voltage) exceeds the maximum common-mode voltage allowed for the operational amplifier in a low-power-supply configuration. Some rail-to-rail input devices have multiple input stages and operate well in this condition, but will transition to a different input stage and introduce an error in the PSRR calculation. In both types of amplifiers, a fixed common-mode voltage can prevent either the common-mode saturation or input stage transition. Keeping a constant common-mode voltage for both measurements of the PSRR test will result in an error that cancels during the calculation of PSRR. The actual common-mode voltage needed for these devices will vary depending on the topology of the amplifier's input stage.

Common-mode rejection ratio

CMRR is the ratio of the differential voltage gain to the common-mode voltage gain. That is, it's the op amp's ability to reject common-mode voltages over a specified range. Because you need the offset voltage to make this measurement, you can use techniques already developed for measuring $V_{os}$ to
In this test procedure, change the input common-mode voltage and measure the change in the op amp's $V_{OS}$. The most direct and obvious way is to apply a common-mode voltage to the DUT's noninverting input. This method requires that the measurement system be referenced to the applied common-mode voltage. Figure 3 shows the test setup for the two-amplifier loop.

You may want to make all measurements with respect to ground. To do that, tie the noninverting input to ground and move the power supplies in a tracking fashion, positively or negatively, to apply effective common-mode voltages to the amplifier. The output must be driven to the midpoint of the supplies to eliminate any $A_{OL}$ errors that corrupt the CMRR measurement. Equations 4 and 5 show how to calculate CMRR.

$$ CMRR = \frac{\Delta V_{input}}{\Delta V_{OS}} $$

Equation 4

$$ CMRR (dB) = 20 \log \left( \frac{\Delta V_{input}}{\Delta V_{OS}} \right) $$

Equation 5

**DC open loop gain**

$A_{OL}$ is the ratio of the output voltage to the differential input voltage. The measurement involves measuring the input offset voltage at several points and calculating $A_{OL}$. 
The procedure for measuring $A_{\text{OL}}$ requires some knowledge of the DUT op amp's output behavior. Ideally, an op amp could swing all the way to both power supply rails. This is not usually the case. $A_{\text{OL}}$ will be specified at some distance from the rails at a given load.

Assume that the output can swing from $V_{\text{OUT}}$ (positive) to $V_{\text{OUT}}$ (negative). If you drive the output to $V_{\text{OUT}}$ (positive), the voltage on the input of the DUT will be $V_{\text{OS}} + V_{\text{IN}}$ (positive). The extra voltage $V_{\text{IN}}$ (positive) is required to drive the output to $V_{\text{OUT}}$ (positive). Conversely, if you drive the output to $V_{\text{OUT}}$ (negative), the voltage on the input of the DUT will change to be $V_{\text{OS}} + V_{\text{IN}}$ (negative). You need to measure that change on the input to achieve the desired full-scale output.

The method to measure $A_{\text{OL}}$ using Figure 1 is:

1. Connect the appropriate load to the DUT.
2. Force $V_{\text{IN}}$ to set $V_{\text{OUT}}$ (positive) to the product data sheet specification for positive swing.
3. Measure $V(1)$, which is: $1001 \times (V_{\text{OS}} + V_{\text{IN}}$ (positive))

   $$\therefore V_{\text{IN}}(\text{pos}) = \frac{V(1)}{1001} \cdot V_{\text{OS}}$$

4. Then, force $V_{\text{IN}}$ to set $V_{\text{OUT}}$ (negative) to the product data sheet specification for negative swing.
5. Measure $V(2)$, which is: $1001 \times (V_{\text{OS}} + V_{\text{IN}}$ (negative))

   $$\therefore V_{\text{IN}}(\text{neg}) = \frac{V(2)}{1001} \cdot V_{\text{OS}}$$

6. Calculate:

   $$A_{\text{OL}} = 20 \times \log \left( \frac{V_{\text{OUT}}(\text{pos}) - V_{\text{OUT}}(\text{neg})}{V_{\text{IN}}(\text{pos}) - V_{\text{IN}}(\text{neg})} \right)$$
7. Substitute the values measured for $V_{\text{IN}}$ (positive) and $V_{\text{IN}}$ (negative).

\[ A_{\text{ol}} = 20 \times \log \left\{ \frac{V_{\text{out}(\text{pos})} - V_{\text{out}(\text{neg})}}{\frac{V(1)}{1001} - V_{\text{os}} - \left( \frac{V(2)}{1001} - V_{\text{os}} \right)} \right\} \]

8. Note that $V_{\text{os}}$ drops out of the equation.

\[ A_{\text{ol}} = 20 \times \log \left\{ \frac{V_{\text{out}(\text{pos})} - V_{\text{out}(\text{neg})}}{\frac{V(1)}{1001} - \frac{V(2)}{1001}} \right\} \]

In a future article, we'll cover input bias-current testing and sources of errors to consider when designing and testing op amps. We'll provide a test circuit that you can use to combine the self-test circuit and two-amplifier loop to take advantage of both test methods. A third article will cover compensation issues because the two amplifier loop will oscillate if not properly compensated.

**References**


**For further reading**

National Semiconductor published test methods for operational amplifiers in their *Linear Edge*
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