The basics of testing op amps, part 2: Test op amps for input bias current

Martin Rowe - February 06, 2012

In part 1 of this series, "Circuits test key op amp parameters," we addressed some of the basic op amp (operational amplifier) tests such as $V_{OS}$ (offset voltage), CMRR (common-mode rejection ratio), PSSR (power-supply rejection ratio), and $A_{ol}$ (amplifier open-loop gain). In this article, we discuss two methods for testing input bias current. The method we choose depends on the magnitude of the bias current. We'll present the sources of errors that you should consider when testing the devices. The next installment of this series will cover a configurable test circuit that lets you make all of the measurements described in this installment.

Data sheets often provide a table of bias currents for an op amp's noninverting and inverting inputs, $i_{B+}$ and $i_{B-}$, respectively. The difference between these two inputs is the input offset current, $I_{OS}$. On the bench, you might be tempted to test the positive input bias current by using the circuit in Figure 1a because the amplifier in this configuration is stable, which will work.
Unfortunately, there is no simple way to keep the amplifier stable while measuring the negative input bias current. Adding a loop amplifier will, though, keep the DUT (device under test) stable, letting you use an electrometer to measure bias current. See the circuit in **Figure 1b**. This circuit is the same two-amplifier test loop that we used to test $V_{OS}$ in part 1, but with a different hook-up.

We just flipped the inputs on both amplifiers to keep the DUT stable. While this technique works well for bench testing, electrometers are too slow for use in high-speed production testing. The method we used in production testing is a modification of the $V_{OS}$ test. To test $I_B$ (input-bias current), we added relays and either resistors or capacitors to the circuit. See the resistors, designated $R_b$, in **Figure 1c**.

For the purpose of this discussion, we describe this test using the two-op-amp test loop. Nevertheless, this technique is equally applicable to the two test loops presented in Part 1. We added a relay and resistor to each input of the DUT in Figure 1c.

With relays K2, and K3 closed, we measure and store the value of $V_{OUT}$ using the $V_{OS}$ measurement technique presented in Part 1. **Equation 1** defines $V_{OUT}$ as a function of $R_{IN}$, $R_f$, and $V_{OS}$.
We rearrange **Equation 1** to get $V_{\text{OS}}$ in **Equation 2**.

$$V_{\text{OS}} = \frac{V_{\text{OUT}}}{\left(\frac{R_{\text{in}} + R_f}{R_{\text{in}}}\right)}$$  \hspace{1cm} \text{Equation 2}$$

Next, we open K2 and make another measurement, which we store as $V_{\text{OUT}}(I_B)$. The measured voltage is caused by the offset voltage of the DUT plus the input bias current flowing through the resistor $R_B$, expressed in **Equation 3**.

$$V_{\text{OUT}}(I_{\text{B-}}) = \left(\frac{R_{\text{IN}} + R_f}{R_{\text{IN}}}\right) \times \left[ V_{\text{OS}} + (I_{\text{B-}} \times R_B) \right]$$  \hspace{1cm} \text{Equation 3}$$

We now solve for $I_{\text{B-}}$ by dividing both sides of the equation by $(R_{\text{IN}} + R_f)/R_{\text{IN}}$ to get **Equation 4**.

$$\frac{V_{\text{OUT}}(I_{\text{B-}})}{\left(\frac{R_{\text{IN}} + R_f}{R_{\text{IN}}}\right)} = \left( V_{\text{OS}} + (I_{\text{B-}} \times R_B) \right)$$  \hspace{1cm} \text{Equation 4}$$

Then, subtract the DUT offset voltage from both sides of **Equation 4** to get **Equation 5**.
\[
\left( \frac{V_{OUT}(I_{B-})}{R_{IN}+R_F} \right) - V_{OS} = I_{B-} \times R_B
\]

Equation 5

Finally, divide both sides of Equation 5 by \( R_B \) to calculate the value of \( I_{B-} \).

\[
I_{B-} = \left( \frac{V_{OUT}(I_{B-})}{R_{IN}+R_F} \right) - V_{OS} \times R_B
\]

Equation 6

You can use a similar technique to measure \( I_{B+} \). To measure \( I_{B+} \), leave K3 closed and open K2. To measure \( I_{B-} \), close K2 and open K3. Because we already measured and know the op amp's \( V_{OS} \), the rest is just math. This result is fairly easy to obtain and requires only a good DMM (digital multimeter).

Note that using a resistor to develop a voltage difference to measure \( I_B \) only works well for bias currents down to a few hundred picoamps. We use a different technique for lower bias currents.

For values of \( I_B \) less than a few hundred picoamps, we use capacitors in place of the \( R_B \) resistors. Once the shorting relay is opened, the bias current causes the loop to integrate at a rate of \( I_C = C(dV/dt) \times \text{loopgain} \). By making measurements at a known time interval, you can calculate the bias current. This method can measure bias current less than 1 pA.

The PCB layout is critical for these really low \( I_B \) currents. Take care to reduce stray capacitance, which might rob some of the \( I_B \) current. Leakage to the input pins of the DUT on the PCB will also cause an error, so create guard rings around the input pins and connect the guards to ground. This will reduce any leakage from high-voltage nodes. From a topology standpoint, replace the \( R_B \) resistors in Figure 1c with low-leakage, temperature-stable capacitors.

Using the capacitive method requires a good clock. That's because input bias current measurement involves opening relays across capacitors connected to the input of the DUT and measuring the voltage change over a known interval. We calculate the input bias current from the measured change in the loop output voltage during a precisely determined period of time.

When the relay across the capacitor opens at \( t_0 \), the output starts to integrate in a positive or negative direction depending on the polarity of the bias current (Figure 2). A programmed delay
lets the circuit to settle down. Then at $t_1$, The DMM takes samples at a known sample rate. This is followed at $t_2$ and by another delay. Finally, at $t_3$, the DMM takes additional samples.

![Diagram of voltage measurement](image)

**Figure 2.** For bias current measurements less than a few hundred picoamps, use capacitors the circuit and take a series of samples with a multimeter. Click on image to enlarge

Maintain a constant duration of the sampling measurement. This way, you know the value of $dt$. Take the average value of the second set of sample measurements and subtract the average value of the first set of sample measurements, which gives the value of $dV$, or change in voltage during time $dt$. You can express the current through a capacitor as:

$$i = C \times \frac{dV}{dt}$$  \hspace{1cm} \text{Equation 7}

Bias current is then calculated by the following equation:

$$I_B = C \times \frac{\text{delta } V \text{ / loop Gain}}{\tau_3 - \tau_1}$$  \hspace{1cm} \text{Equation 8}

**Typical error sources**

No discussion of $V_{os}$ measurement is complete without a discussion about the source of errors that will be encountered in making the measurement. The obvious errors are those caused by the DMM's resolution and by the component values chosen (noise and tolerance), especially for resistors. More subtle errors come in three types:

A. Thermally generated electromotive forces (emfs) caused by: Relay contact

   - Solder joints
• Inter-board pin connections
• Automated test handler contacts and sockets

B. Leakage currents caused by:
• Power supplies
• Relay control and supply traces
• Properties of PCB materials

C. Noise
• Environment
• Testers
• Components
• The DUT’s themselves

Typical sources of error in all of the DUT configurations discussed here are thermally generated emfs and leakage currents. Leakage current primarily affects bias current measurements, whereas thermally generated emfs affect all low-level offset measurements. Minimizing these effects is necessary to ensure system capability and measurement accuracy.

Leakage currents are caused by surface contamination and resistive paths through components or in the PCB material. Surface contamination usually can be controlled with thorough board cleaning, but humidity may change the surface leakage currents. Other resistive paths are set by the isolation resistance of the materials. Leakage current may also occur when the resistive path leads to power-supply lines or to relay-control-and-supply lines. Some of these leakage paths can be mitigated by using guard rings, and latching relays with active high drivers.

Thermal emfs are generated in relay contacts, solder joints, inter-board pin connections, and all other test handler contacts and sockets. Consider, for example, the $V_{OS}$ two-amplifier measurement circuit shown in Figure 1c. Leakage currents won't significantly affect this measurement. But, this circuit fails to show the many sources of thermal emf (electromotive force) errors.

**Figure 3** shows the sources of error caused by thermal emfs, labeled VT. For room-temperature measurements, the gradients aren't exceptional. But, when testing in cold or hot environments, the thermal gradients from the DUT to the resistors and relays can be significant.
Part 3 of this series will discuss design considerations for the test boards.

For further reading

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