Quasistatic Spice model targets ceramic capacitors with Y5V dielectric

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Ceramic Y5V SMT capacitors have recently become available in values and sizes that were previously available only with electrolytic capacitors. At first glance, they may seem a worthwhile unpolarized alternative to electrolytic capacitors, and they sometimes are. These capacitors, however, have a capacitance that is a function of the applied voltage. Modeling them as ordinary linear capacitors can lead to great discrepancies between simulated and measured—let alone expected—results.

**Figure 1** shows some measurements of capacitance as a function of dc voltage on a 10-μF, 25V Y5V 1206 capacitor. **Reference 1** describes a method of modeling nonlinear capacitors using a look-up table. The use of a look-up table, however, adds complexity to the simulation and can lead to convergence problems. If you limit the operating voltage to approximately 80% of the capacitor’s voltage rating, you may find that a simpler quadratic quasistatic model can be sufficient for quickly arriving at a first approximation.
Fitting the measured data of $C$ to $a_0 + (a_1 V_{DC}) + (a_2 V_{DC}^2)$ using quadratic regression yields the coefficients of $8.500065 \times 10^{-6}$, $-7.445791 \times 10^{-7}$, and $1.922001 \times 10^{-8}$ for $a_0$, $a_1$, and $a_2$, respectively. **Listing 1** shows the conversion from the parameters to the nonlinear-capacitor model in PSpice. You can see the equivalent capacity in PSpice’s graphical postprocessor Probe as $i(c)/(2 \times 3.14159 \times \text{frequency})$.

The differences between the measured values and the quadratic approximation are at worst approximately 20% (**Figure 2**). The relative residues are normally distributed with a mean of 2.5% and a standard deviation of 10%. Those deviations might seem to be a rough approximation for a model, but you must compare them with the normal linear C model, for which the relative error at 50% of the dc-voltage rating is already approximately 300%. Note that in practical applications you must limit the capacitor terminal voltage to no more than 80% of the capacitor rating so that the model almost always gives a better approximation than the worst-case value might suggest.

**Listing 1 Conversion Parameters**

```plaintext
LISTING 1 CONVERSION PARAMETERS
quadratic y5v-cap model
  .param a0=8.500065u
  .param a1=-744.5791n
  .param a2=19.22001n
  .param valdc=1
  c1 0 cmd [a0]
  vin 0 dc [valdc] ac 1
  .model cmdcap
    (c1=1 vc1=[a1/a0]
     vc2=[a2/a0])
  .ac dec 20 100 100k
  .step lin param valdc 0 25 1
  *display equivalent c as
  i(c)/(2*3.14159*frequency)
  .probe
  .end
```

A simple rectifier setup checks the validity of the model (**Figure 3**). It measures a peak-to-peak ripple voltage of 10.2V (**Figure 4**). Simulating the circuit with the quadratic model in PSpice shows a ripple voltage of 10.4V (**Figure 5**). You don’t need PSpice for this model; Spice 2G6 also has a built-in feature for modeling this type of capacitor. You enter it in this format:

```
c1 2 0 poly 8.500065u
   -744.5791n 19.22001n
```

PSpice no longer has this feature, even though it is said to be Spice 2G6-based.
Note that replacing the capacitor with an ordinary electrolytic that has the same capacitance and voltage rating would reduce the ripple voltage to approximately 5 or 6V. That result is not surprising, but it again shows that you can’t just replace an electrolytic capacitor with a ceramic one of the same capacitance and voltage rating.

References

2. Cain, Jeffrey, PhD, “Comparison of multilayer ceramic and tantalum capacitors,” AVX Corp.

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