Thorough test means testing through the RAM

Ron Press - September 17, 2012

Structural test is the foundation of the majority of IC production testing. The idea of structural test is that the entire chip operation doesn’t need to be known. Instead, the structural pieces and their connections are individually verified. This is a very effective approach and enables both high levels of defect detection and automation since the complex IC behavior is broken down into simple pieces. Scan testing verifies the combinational logic and state elements like flip-flops and latches, whereas, memory built-in self test (BIST) is used to test RAM and other memory devices. The problem is that timing defects between the RAM and surrounding logic, often referred to as “shadow logic,” could be missed.

It is easy to miss testing for timing defects between memories and logic. Figure 1 shows a common test approach. Memory BIST will perform at-speed writes and reads through the memory. Scan tests will perform at-speed launch and captures through the flops and random logic. The problem occurs when memory devices are bypassed to simplify scan testing. Bypass logic ports the functional paths around the memories. Scan pattern generation is simplified since the multiple step sequential behavior of the memory is essentially removed from the circuit.

Figure 1. As shown, memory BIST logic bypasses the functional inputs of the RAM and captures at the output. Scan bypass creates artificially long paths around the RAM between scan cells. However, the functional path from flops at the scan cells to and from the memory would not be tested at speed with this configuration.
One method of memory bypass is shown in the figure where the data into the memory is muxed to the data out path. The address signals are sent to scan cells in this example. Another method to bypass the address signals is to XOR them together with data signals at the output side of the memory. This type of bypass setup is fine for stuck-at or static scan testing. However, it creates a problem for at-speed testing. The bypass path is a false path. If it is tested at-speed then functional devices could be discarded. Even if the bypass path is registered and scanned, it is not a real functional path. In this case there isn’t a path to verify the logic from flops through combinational logic to memory. Similarly, a standard approach to memory BIST performs at-speed tests of the memory but it accesses the address and data at the memory and does not utilize the functional paths.

Fortunately, there are a few effective methods available to verify the timing of this logic around the memory. One method is just not to bypass the memory. Automatic test pattern generation (ATPG) tools have several methods to use the memory as a launch and capture point during scan test. The scan tests using the memory will perform writes to two addresses and then read from two addresses to pass fault detection through the surrounding logic and memory to a scan cell capture point.

If the memory can hold state during scan shifting then a multiload pattern can be used. It will perform multiple scan loads but perform at-speed write and read operations to detected ATPG targeted faults. If the memory cannot hold state during shift then a sequential pattern can be used where the ATPG tool determines how to set up a scan load such that several at-speed clock pulses will consecutively perform the write and read operations necessary for at-speed detection of faults around the memories. Since the bypass setup is much easier for ATPG, it makes sense to use it for stuck-at detection.

More memories have become available that use the internal functional logic within the memory as scan wrappers. Thus, at-speed scan testing can directly test the shadow logic using scan cells. The last solution is to move the memory BIST MUX access outside the high-speed shadow logic around the memory. This not only provides detection of timing defects in the shadow logic but also removes any performance impact due to the memory BIST MUXing. This approach is referred to as shared bus memory BIST and was described in a previous article.

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Ron Press is the technical marketing manager of the Silicon Test Solutions products at Mentor Graphics. The 25-year veteran of the test and DFT (design-for-test) industry has presented seminars on DFT and test throughout the world. He has published dozens of papers in the field of test, is a member of the International Test Conference (ITC) Steering Committee, and is a Golden Core member of the IEEE Computer Society, and a Senior Member of IEEE. Press has patents on reduced-pin-count testing and glitch-free clock switching.